Pin Name	503-Pin PGA
MSEL0 (2)	AT40
MSEL1 (2)	AV40
nSTATUS (2)	AY4
nCONFIG (2)	AY40
DCLK (2)	H40
CONF_DONE (2)	F4
INIT_DONE (3)	V6
nCE (2)	K40
nCEO (2)	H4
nWS (4)	A3
nRS (4)	C5
nCS (4)	C1
CS (4)	C3
RDYnBSY (4)	T6
CLKUSR (4)	H6
DATA7 (4)	E29
DATA6 (4)	D30
DATA5 (4)	C31
DATA4 (4)	B32
DATA3 (4)	D32
DATA2 (4)	B34
DATA1 (4)	E33
DATA0 (2), (5)	F40
TDI (2)	M40
TDO (2)	K4
TCK (2)	D4
TMS (2)	AT4
TRST (2)	AV4
Dedicated Inputs	D20, D24, AY24, AY20
Dedicated Clock Pins	D22, AY22
LOCK (12)	AV14
GCLK1 (13)	AY22
DEV_CLRn (3)	F22
DEV_OE (3)	G21
VCCINT	C11, E39, G27, N5, N41, W39, AC3, AG7, AR3, AR41, AU37, AW5, AW25, AW41, BA17
VCCIO	C9, C15, C25, C33, C37, E19, E41, G7, L3, R41, U3, U37, W5, AC41, AE5, AJ41, AL39, AU3, AU17, AW3, AW19, BA9, BA27, BA29, BA37
VCC_CKLK (14)	BA19
GNDINT	C17, E3, E5, E25, G37, J3, J41, U7, AA3, AE39, AL5, AL41, AU27, AW39, BA7, BA13
GNDIO	C21, C23, C39, C41, E13, E31, G3, G17, N3, N39, R3, W3, W41, AA41, AG37, AJ3, AN3, AN41, AU7, AU41, AW13, AW31, BA11, BA23, BA21
GND_CKLK (14)	BA25
No Connect (N.C.)	–
Total User I/O Pins (8)	406

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) The optional JTAG pin TRST is not used in the 100-pin or 144-pin TQFP package.
(7) To maintain pin compatibility when transferring to the EPF10K10 or EPF10K10A device from any other device in the 208-pin PQFP or 256-pin FineLine BGA package, do not use these pins as user I/O pins.
(8) The user I/O pin count includes dedicated input pins, dedicated clock pins, and all I/O pins.
(9) To maintain pin compatibility when transferring to the EPF10K30 device from any other device in the 356-pin BGA or 484-pin FineLine BGA package, do not use these pins as user I/O pins.

(10) To maintain pin compatibility when transferring to the EPF10K50V device from any other device in the 484-pin FineLine BGA package, do not use these pins as user I/O pins.
(11) To maintain pin compatibility when transferring from the EPF10K100 to the EPF10K70 in the 503-pin PGA package, do not use these pins as user I/O pins.
(12) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry are locked to the incoming clock and generate an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(13) This pin drives the ClockLock and ClockBoost circuitry.
(14) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device.
(15) To maintain pin compatibility when transferring to the EPF10K100A device from another device in the 600-pin BGA package, do not use these pins as user I/O pins.
(16) The 240-pin QFP packages do not support the MultiVolt I/O feature so there are no VCCIO pins.