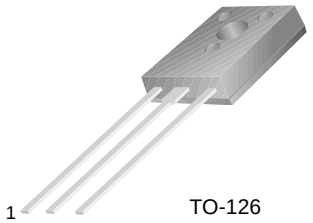
FAIRCHILD
SEMICONDUCTOR TM

# BD135/137/139

## Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively



1

TO-126

1. Emitter 2.Collector 3.Base

## NPN Epitaxial Silicon Transistor

### Absolute Maximum Ratings $T_C$=25°C unless otherwise noted

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{CBO}$ | Collector-Base Voltage : BD135 | 45 | V |
| | : BD137 | 60 | V |
| | : BD139 | 80 | V |
| $V_{CEO}$ | Collector-Emitter Voltage : BD135 | 45 | V |
| | : BD137 | 60 | V |
| | : BD139 | 80 | V |
| $V_{EBO}$ | Emitter-Base Voltage | 5 | V |
| $I_C$ | Collector Current (DC) | 1.5 | A |
| $I_{CP}$ | Collector Current (Pulse) | 3.0 | A |
| $I_B$ | Base Current | 0.5 | A |
| $P_C$ | Collector Dissipation ($T_C$=25°C) | 12.5 | W |
| $P_C$ | Collector Dissipation ($T_a$=25°C) | 1.25 | W |
| $T_J$ | Junction Temperature | 150 | °C |
| $T_{STG}$ | Storage Temperature | - 55 ~ 150 | °C |

### Electrical Characteristics $T_C$=25°C unless otherwise noted

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CEO}$(sus) | Collector-Emitter Sustaining Voltage | | | | | |
| | : BD135 | $I_C$ = 30mA, $I_B$ = 0 | 45 | | | V |
| | : BD137 | | 60 | | | V |
| | : BD139 | | 80 | | | V |
| $I_{CBO}$ | Collector Cut-off Current | $V_{CB}$ = 30V, $I_E$ = 0 | | | 0.1 | µA |
| $I_{EBO}$ | Emitter Cut-off Current | $V_{EB}$ = 5V, $I_C$ = 0 | | | 10 | µA |
| $h_{FE1}$ | DC Current Gain : ALL DEVICE | $V_{CE}$ = 2V, $I_C$ = 5mA | 25 | | | |
| $h_{FE2}$ | : ALL DEVICE | $V_{CE}$ = 2V, $I_C$ = 0.5A | 25 | | | |
| $h_{FE3}$ | : BD135 | $V_{CE}$ = 2V, $I_C$ = 150mA | 40 | | 250 | |
| | : BD137, BD139 | | 40 | | 160 | |
| $V_{CE}$(sat) | Collector-Emitter Saturation Voltage | $I_C$ = 500mA, $I_B$ = 50mA | | | 0.5 | V |
| $V_{BE}$(on) | Base-Emitter ON Voltage | $V_{CE}$ = 2V, $I_C$ = 0.5A | | | 1 | V |

### $h_{FE}$ Classification

| Classification | 6 | 10 | 16 |
|---|---|---|---|
| $h_{FE3}$ | 40 ~ 100 | 63 ~ 160 | 100 ~ 250 |

# Typical Characteristics

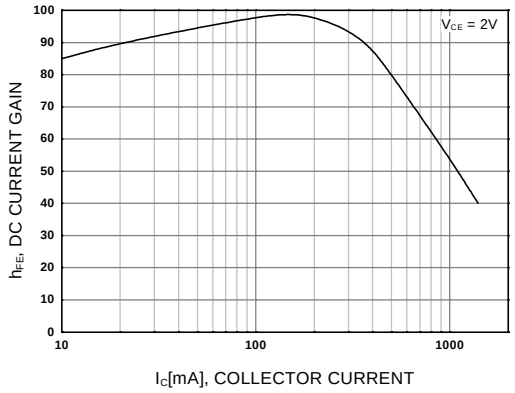



**Figure 1. DC current Gain**

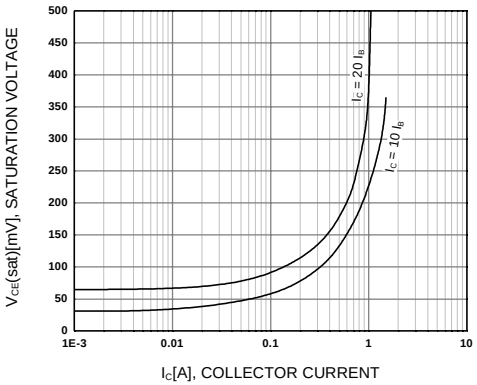



**Figure 2. Collector-Emitter Saturation Voltage**

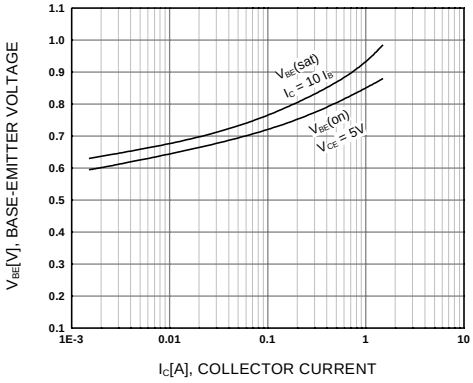



**Figure 3. Base-Emitter Voltage**

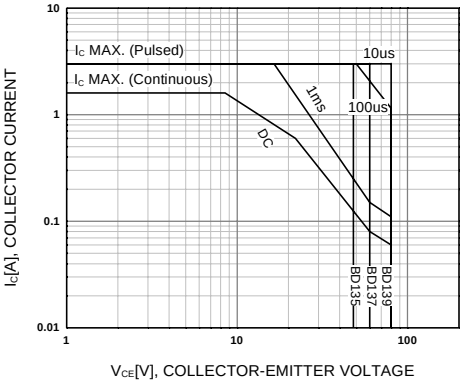



**Figure 4. Safe Operating Area**

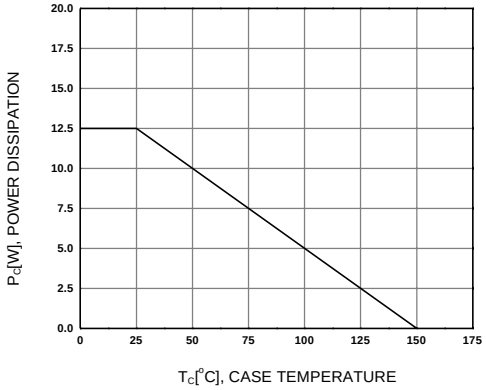
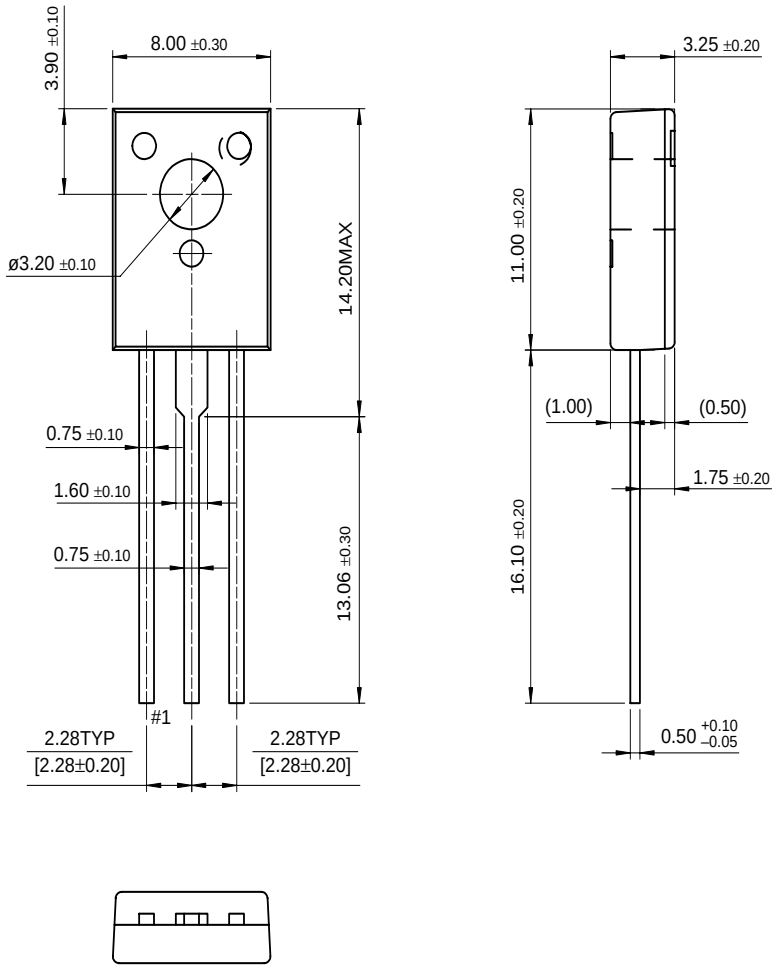



**Figure 5. Power Derating**

## Package Demensions

TO-126




Dimensions in Millimeters

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|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
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| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

# HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

ADE-207-272(Z)
'99.9
Rev. 0.0

## Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7V to 5.5V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

## Features

- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
  — 2.7 to 5.5V
- Wide range of liquid crystal display driver power
  — 3.0 to 11V
- Liquid crystal drive waveform
  — A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  — 2 MHz (when $V_{CC}$ = 5V)
- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  — 208 character fonts (5 × 8 dot)
  — 32 character fonts (5 × 10 dot)

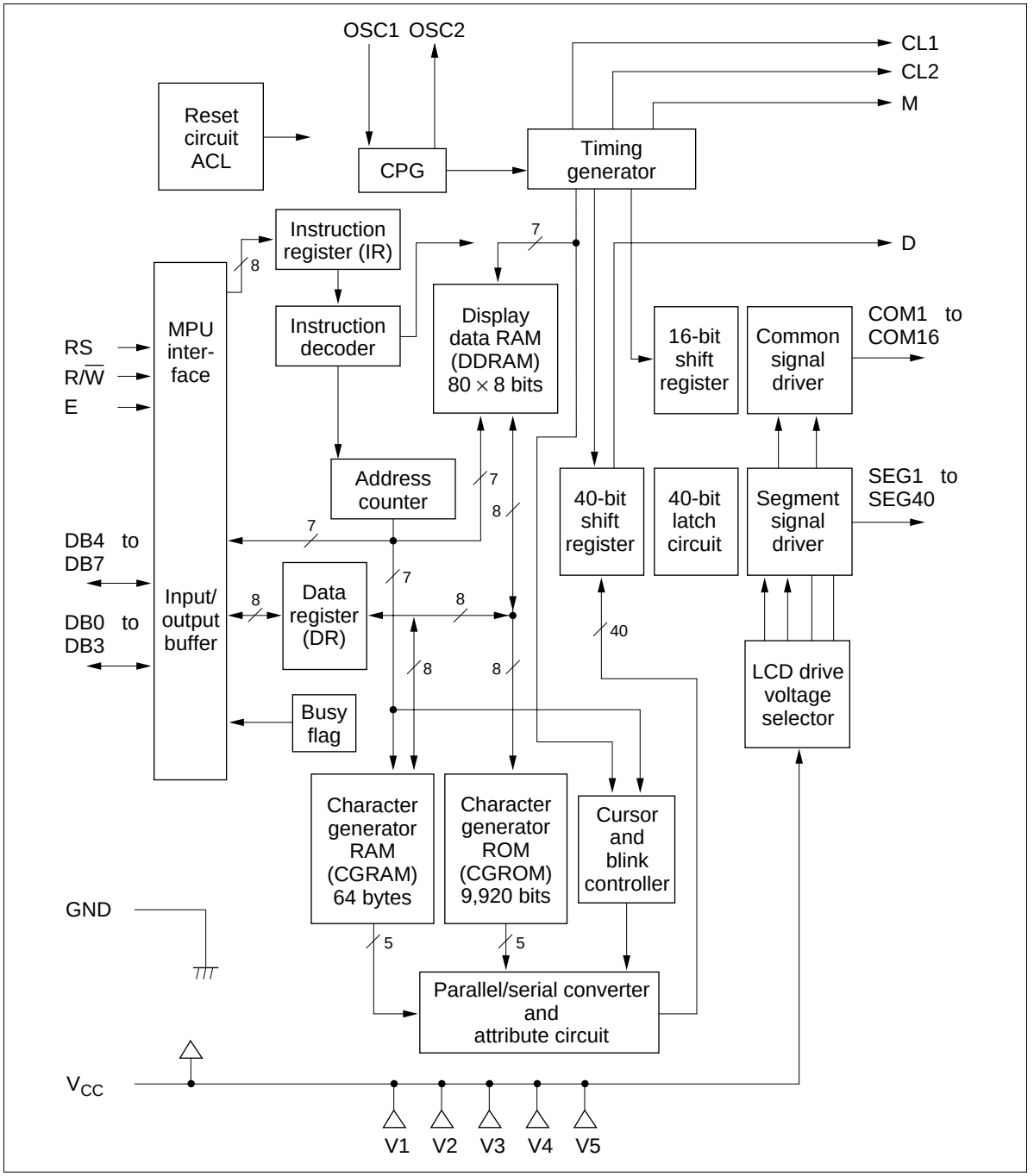
- 64 × 8-bit character generator RAM
  - — 8 character fonts (5 × 8 dot)
  - — 4 character fonts (5 × 10 dot)
- 16-common × 40-segment liquid crystal display driver
- Programmable duty cycles
  - — 1/8 for one line of 5 × 8 dots with cursor
  - — 1/11 for one line of 5 × 10 dots with cursor
  - — 1/16 for two lines of 5 × 8 dots with cursor
- Wide range of instruction functions:
  - — Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- Pin function compatibility with HD44780S
- Automatic reset circuit that initializes the controller/driver after power on
- Internal oscillator with external resistors
- Low power consumption

## Ordering Information

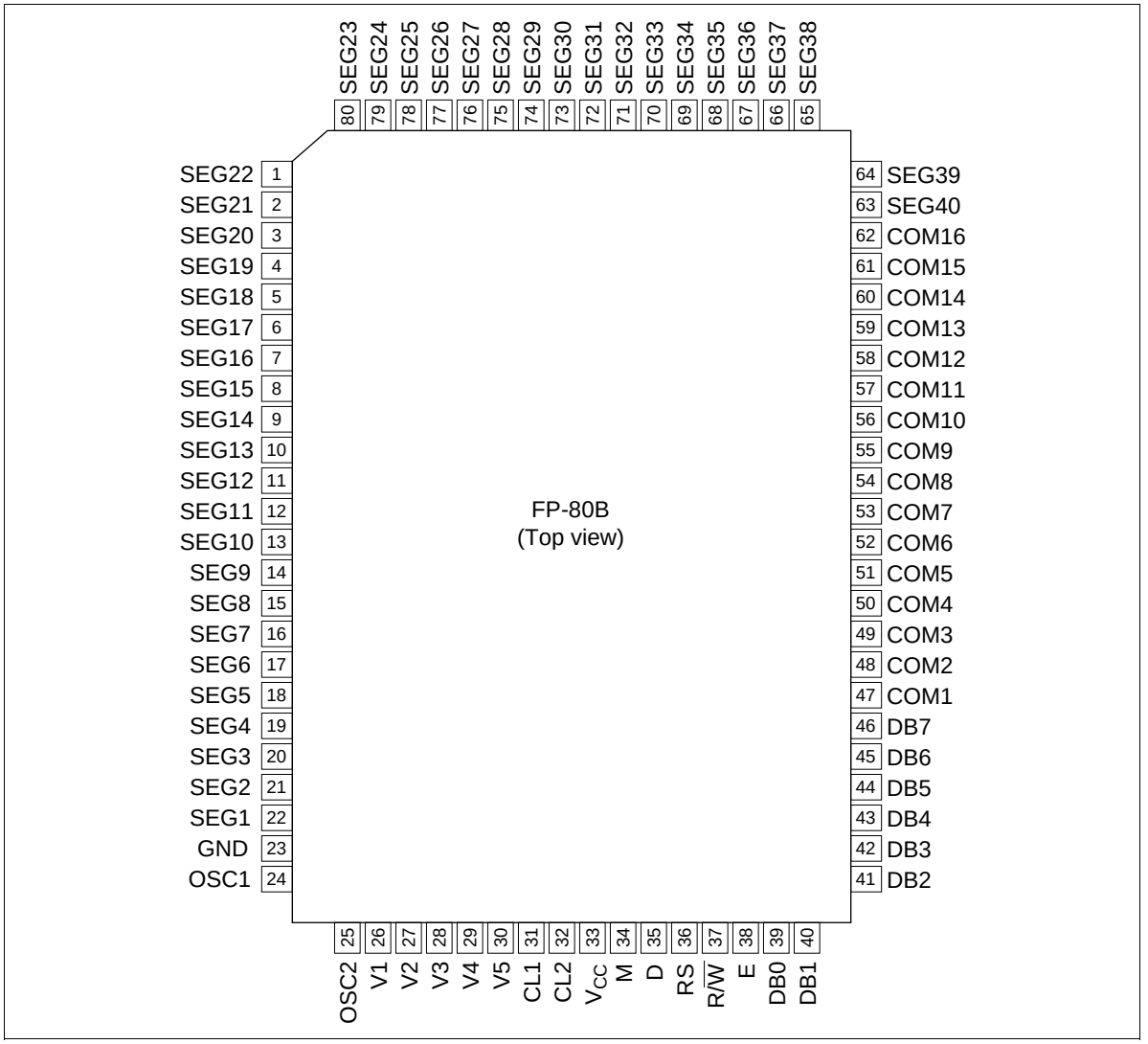
| Type No. | Package | CGROM |
|---|---|---|
| HD44780UA00FS | FP-80B | Japanese standard font |
| HCD44780UA00 | Chip | |
| HD44780UA00TF | TFP-80F | |
| HD44780UA02FS | FP-80B | European standard font |
| HCD44780UA02 | Chip | |
| HD44780UA02TF | TFP-80F | |
| HD44780UBxxFS | FP-80B | Custom font |
| HCD44780UBxx | Chip | |
| HD44780UBxxTF | TFP-80F | |

Note: xx: ROM code No.

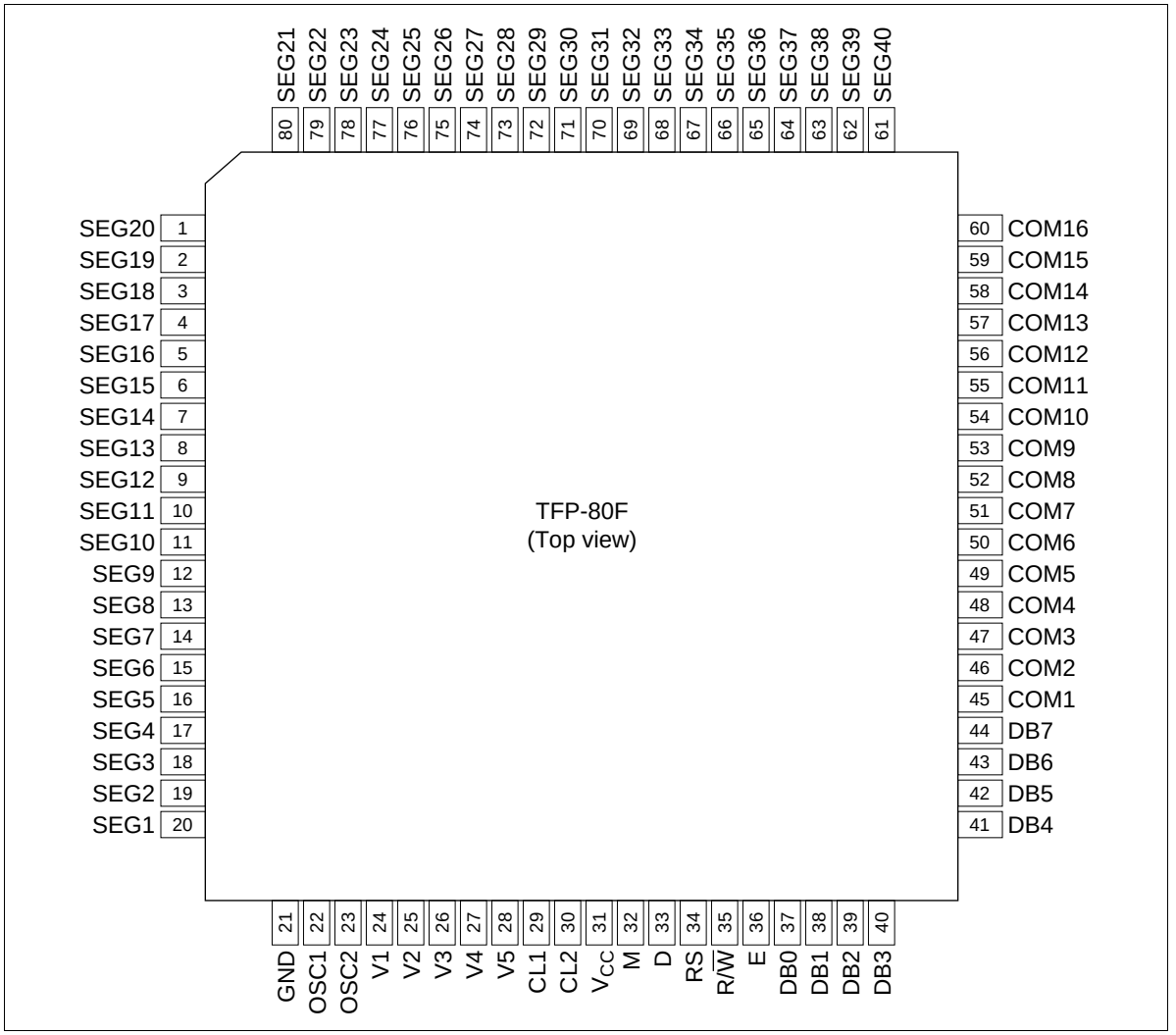
## HD44780U Block Diagram



## HD44780U Pin Arrangement (FP-80B)

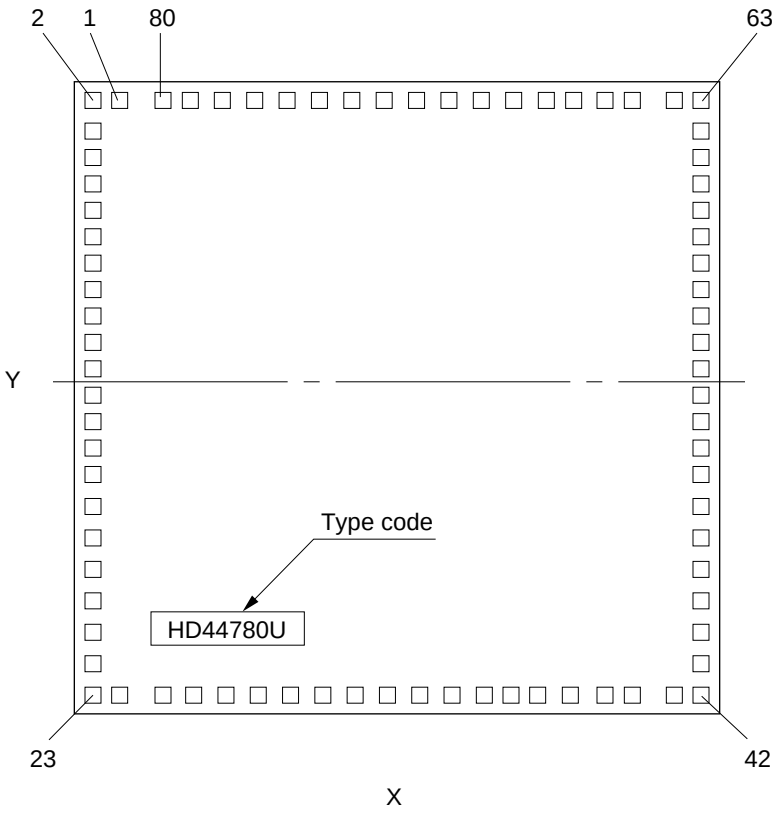


## HD44780U Pin Arrangement (TFP-80F)



## HD44780U Pad Arrangement

Chip size: $4.90 \times 4.90$ mm$^2$
Coordinate: Pad center (μm)
Origin: Chip center
Pad size: $114 \times 114$ μm$^2$



## HCD44780U Pad Location Coordinates

| | | Coordinate | | | | Coordinate | |
|---|---|---|---|---|---|---|---|
| Pad No. | Function | X (um) | Y (um) | Pad No. | Function | X (um) | Y (um) |
| 1 | SEG22 | –2100 | 2313 | 41 | DB2 | 2070 | –2290 |
| 2 | SEG21 | –2280 | 2313 | 42 | DB3 | 2260 | –2290 |
| 3 | SEG20 | –2313 | 2089 | 43 | DB4 | 2290 | –2099 |
| 4 | SEG19 | –2313 | 1833 | 44 | DB5 | 2290 | –1883 |
| 5 | SEG18 | –2313 | 1617 | 45 | DB6 | 2290 | –1667 |
| 6 | SEG17 | –2313 | 1401 | 46 | DB7 | 2290 | –1452 |
| 7 | SEG16 | –2313 | 1186 | 47 | COM1 | 2313 | –1186 |
| 8 | SEG15 | –2313 | 970 | 48 | COM2 | 2313 | –970 |
| 9 | SEG14 | –2313 | 755 | 49 | COM3 | 2313 | –755 |
| 10 | SEG13 | –2313 | 539 | 50 | COM4 | 2313 | –539 |
| 11 | SEG12 | –2313 | 323 | 51 | COM5 | 2313 | –323 |
| 12 | SEG11 | –2313 | 108 | 52 | COM6 | 2313 | –108 |
| 13 | SEG10 | –2313 | –108 | 53 | COM7 | 2313 | 108 |
| 14 | SEG9 | –2313 | –323 | 54 | COM8 | 2313 | 323 |
| 15 | SEG8 | –2313 | –539 | 55 | COM9 | 2313 | 539 |
| 16 | SEG7 | –2313 | –755 | 56 | COM10 | 2313 | 755 |
| 17 | SEG6 | –2313 | –970 | 57 | COM11 | 2313 | 970 |
| 18 | SEG5 | –2313 | –1186 | 58 | COM12 | 2313 | 1186 |
| 19 | SEG4 | –2313 | –1401 | 59 | COM13 | 2313 | 1401 |
| 20 | SEG3 | –2313 | –1617 | 60 | COM14 | 2313 | 1617 |
| 21 | SEG2 | –2313 | –1833 | 61 | COM15 | 2313 | 1833 |
| 22 | SEG1 | –2313 | –2073 | 62 | COM16 | 2313 | 2095 |
| 23 | GND | –2280 | –2290 | 63 | SEG40 | 2296 | 2313 |
| 24 | OSC1 | –2080 | –2290 | 64 | SEG39 | 2100 | 2313 |
| 25 | OSC2 | –1749 | –2290 | 65 | SEG38 | 1617 | 2313 |
| 26 | V1 | –1550 | –2290 | 66 | SEG37 | 1401 | 2313 |
| 27 | V2 | –1268 | –2290 | 67 | SEG36 | 1186 | 2313 |
| 28 | V3 | –941 | –2290 | 68 | SEG35 | 970 | 2313 |
| 29 | V4 | –623 | –2290 | 69 | SEG34 | 755 | 2313 |
| 30 | V5 | –304 | –2290 | 70 | SEG33 | 539 | 2313 |
| 31 | CL1 | –48 | –2290 | 71 | SEG32 | 323 | 2313 |
| 32 | CL2 | 142 | –2290 | 72 | SEG31 | 108 | 2313 |
| 33 | $V_{CC}$ | 309 | –2290 | 73 | SEG30 | –108 | 2313 |
| 34 | M | 475 | –2290 | 74 | SEG29 | –323 | 2313 |
| 35 | D | 665 | –2290 | 75 | SEG28 | –539 | 2313 |
| 36 | RS | 832 | –2290 | 76 | SEG27 | –755 | 2313 |
| 37 | R/$\overline{W}$ | 1022 | –2290 | 77 | SEG26 | –970 | 2313 |
| 38 | E | 1204 | –2290 | 78 | SEG25 | –1186 | 2313 |
| 39 | DB0 | 1454 | –2290 | 79 | SEG24 | –1401 | 2313 |
| 40 | DB1 | 1684 | –2290 | 80 | SEG23 | –1617 | 2313 |

## Pin Functions

| Signal | No. of Lines | I/O | Device Interfaced with | Function |
|---|---|---|---|---|
| RS | 1 | I | MPU | Selects registers.<br>0: Instruction register (for write) Busy flag: address counter (for read)<br>1: Data register (for write and read) |
| R/$\overline{W}$ | 1 | I | MPU | Selects read or write.<br>0: Write<br>1: Read |
| E | 1 | I | MPU | Starts data read/write. |
| DB4 to DB7 | 4 | I/O | MPU | Four high order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U. DB7 can be used as a busy flag. |
| DB0 to DB3 | 4 | I/O | MPU | Four low order bidirectional tristate data bus pins. Used for data transfer and receive between the MPU and the HD44780U.<br>These pins are not used during 4-bit operation. |
| CL1 | 1 | O | Extension driver | Clock to latch serial data D sent to the extension driver |
| CL2 | 1 | O | Extension driver | Clock to shift serial data D |
| M | 1 | O | Extension driver | Switch signal for converting the liquid crystal drive waveform to AC |
| D | 1 | O | Extension driver | Character pattern data corresponding to each segment signal |
| COM1 to COM16 | 16 | O | LCD | Common signals that are not used are changed to non-selection waveforms. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor. |
| SEG1 to SEG40 | 40 | O | LCD | Segment signals |
| V1 to V5 | 5 | — | Power supply | Power supply for LCD drive<br>$V_{CC}$ –V5 = 11 V (max) |
| $V_{CC}$, GND | 2 | — | Power supply | $V_{CC}$: 2.7V to 5.5V, GND: 0V |
| OSC1, OSC2 | 2 | — | Oscillation resistor clock | When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1. |

## Function Description

### Registers

The HD44780U has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator RAM (CGRAM). The IR can only be written from the MPU.

The DR temporarily stores data to be written into DDRAM or CGRAM and temporarily stores data to be read from DDRAM or CGRAM. Data written into the DR from the MPU is automatically written into DDRAM or CGRAM by an internal operation. The DR is also used for data storage when reading data from DDRAM or CGRAM. When address information is written into the IR, data is read and then stored into the DR from DDRAM or CGRAM by an internal operation. Data transfer between the MPU is then completed when the MPU reads the DR. After the read, data in DDRAM or CGRAM at the next address is sent to the DR for the next read from the MPU. By the register selector (RS) signal, these two registers can be selected (Table 1).

### Busy Flag (BF)

When the busy flag is 1, the HD44780U is in the internal operation mode, and the next instruction will not be accepted. When RS = 0 and R/$\overline{W}$ = 1 (Table 1), the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the AC. Selection of either DDRAM or CGRAM is also determined concurrently by the instruction.

After writing into (reading from) DDRAM or CGRAM, the AC is automatically incremented by 1 (decremented by 1). The AC contents are then output to DB0 to DB6 when RS = 0 and R/$\overline{W}$ = 1 (Table 1).

**Table 1 Register Selection**

| RS | R/$\overline{W}$ | Operation |
|---|---|---|
| 0 | 0 | IR write as an internal operation (display clear, etc.) |
| 0 | 1 | Read busy flag (DB7) and address counter (DB0 to DB6) |
| 1 | 0 | DR write as an internal operation (DR to DDRAM or CGRAM) |
| 1 | 1 | DR read as an internal operation (DDRAM or CGRAM to DR) |

**Display Data RAM (DDRAM)**

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address ($A_{DD}$) is set in the address counter (AC) as hexadecimal.

- 1-line display (N = 0) (Figure 2)
  - When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the HD44780, 8 characters are displayed. See Figure 3.

    When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

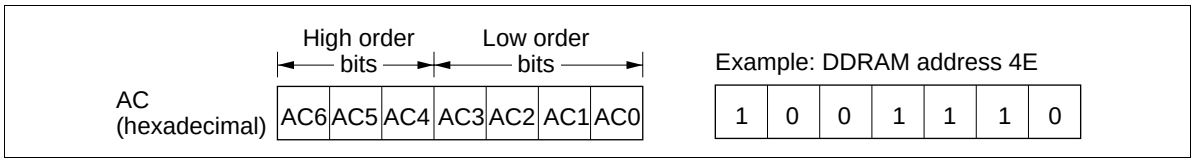



**Figure 1 DDRAM Address**

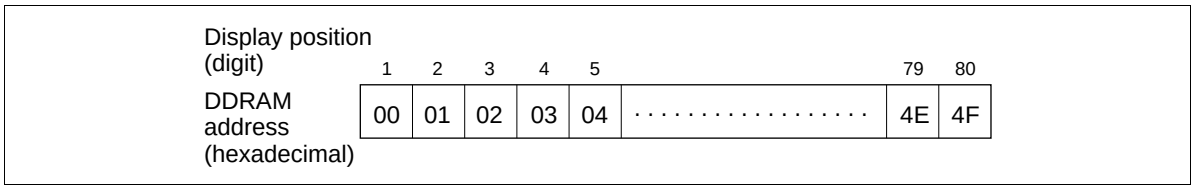



**Figure 2 1-Line Display**

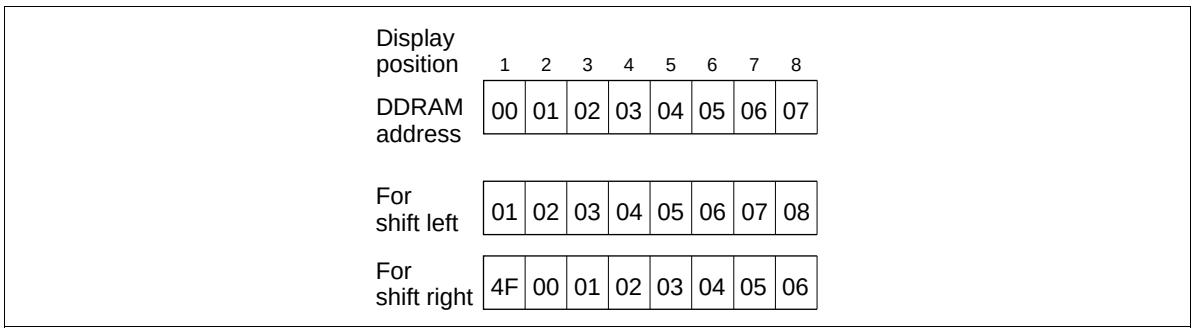



**Figure 3 1-Line by 8-Character Display Example**

- 2-line display (N = 1) (Figure 4)

  — Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the HD44780 is used, 8 characters × 2 lines are displayed. See Figure 5.

  When display shift operation is performed, the DDRAM address shifts. See Figure 5.

| Display position | 1 | 2 | 3 | 4 | 5 | | 39 | 40 |
|---|---|---|---|---|---|---|---|---|
| DDRAM address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | · · · · · · · · · · · · · · · · · · | 26 | 27 |
| | 40 | 41 | 42 | 43 | 44 | · · · · · · · · · · · · · · · · · · | 66 | 67 |

**Figure 4 2-Line Display**

| Display position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| DDRAM address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| For shift left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| For shift right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 |

**Figure 5 2-Line by 8-Character Display Example**

— Case 2: For a 16-character × 2-line display, the HD44780 can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

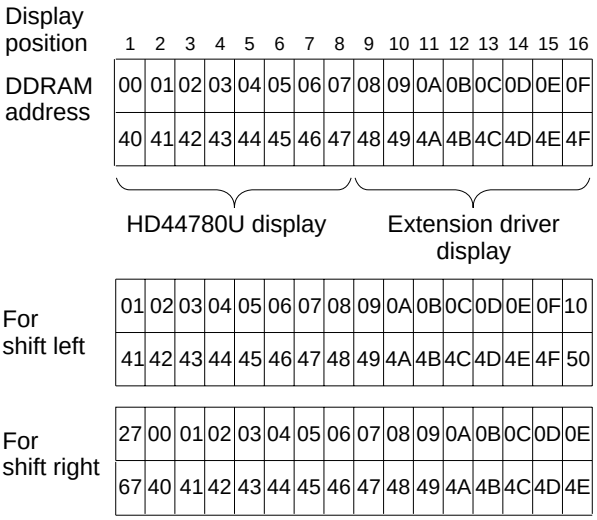



**Figure 6 2-Line by 16-Character Display Example**

### Character Generator ROM (CGROM)

The character generator ROM generates 5 × 8 dot or 5 × 10 dot character patterns from 8-bit character codes (Table 4). It can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

### Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5 × 8 dots, eight character patterns can be written, and for 5 × 10 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns.

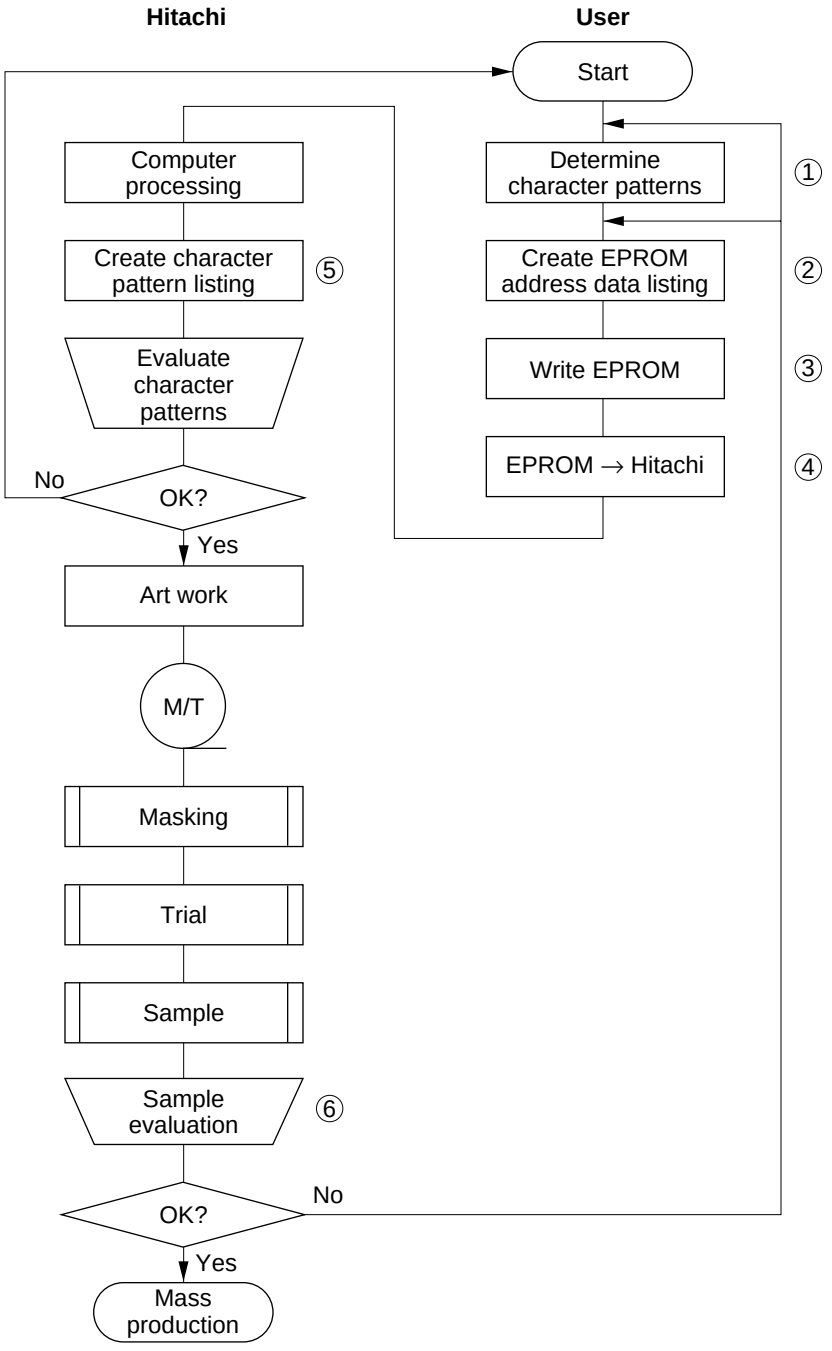
Areas that are not used for display can be used as general data RAM.

### Modifying Character Patterns

- Character pattern development procedure

The following operations correspond to the numbers listed in Figure 7:

1. Determine the correspondence between character codes and character patterns.
2. Create a listing indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into the EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing on the EPROM is performed at Hitachi to create a character pattern listing, which is sent to the user.
6. If there are no problems within the character pattern listing, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When it is confirmed by the user that the character patterns are correctly written, mass production of the LSI proceeds at Hitachi.




Note: For a description of the numbers used in this figure, refer to the preceding page.

**Figure 7 Character Pattern Development Procedure**

- Programming character patterns

  This section explains the correspondence between addresses and data used to program character patterns in EPROM. The HD44780U character generator ROM can generate 208 5 × 8 dot character patterns and 32 5 × 10 dot character patterns for a total of 240 different character patterns.

  — Character patterns

  EPROM address data and character pattern data correspond with each other to form a 5 × 8 or 5 × 10 dot character pattern (Tables 2 and 3).

**Table 2 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 8 Dots)**

| EPROM Address | | | | | | | | | | | | | Data | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | O4 | O3 | O2 | O1 | LSB O0 | |
| | | | | | | | | 0 | 0 | 0 | 0 | | 1 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 0 | 0 | 1 | 0 | | 1 | 0 | 1 | 1 | 0 | |
| | | | | | | | | 0 | 0 | 1 | 1 | | 1 | 1 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 1 | 0 | 0 | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 1 | 0 | 1 | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 1 | 1 | 0 | | 1 | 1 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | ← Cursor position |
| | | | | | | | | 1 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 0 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 0 | 1 | 0 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 0 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 1 | 0 | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 1 | 1 | | 0 | 0 | 0 | 0 | 0 | |

Character code — Line position

Notes:
1. EPROM addresses A11 to A4 correspond to a character code.
2. EPROM addresses A3 to A0 specify a line position of the character pattern.
3. EPROM data O4 to O0 correspond to character pattern data.
4. EPROM data O5 to O7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 9 and the following lines must be blanked with 0s for a 5 × 8 dot character fonts.

— Handling unused character patterns

1. EPROM data outside the character pattern area: Always input 0s.
2. EPROM data in CGRAM area: Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)
3. EPROM data used when the user does not use any HD44780U character pattern: According to the user application, handled in one of the two ways listed as follows.
   a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)
   b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

**Table 3 Example of Correspondence between EPROM Address Data and Character Pattern (5 × 10 Dots)**

| EPROM Address | | | | | | | | | | | | Data | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | O4 | O3 | O2 | O1 | LSB O0 | |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | |
| | | | | | | | | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | |
| | | | | | | | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | |
| | | | | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | |
| | | | | | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | ← Cursor position |
| | | | | | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |

Character code

Line position

Notes: 1. EPROM addresses A11 to A3 correspond to a character code.
2. EPROM addresses A3 to A0 specify a line position of the character pattern.
3. EPROM data O4 to O0 correspond to character pattern data.
4. EPROM data O5 to O7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 11 and the following lines must be blanked with 0s for a 5 × 10 dot character fonts.

**Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A00)**

| Upper 4 Bits / Lower 4 Bits | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| xxxx0000 | CG RAM (1) | | | | | | | | | | | | | | | |
| xxxx0001 | (2) | | | | | | | | | | | | | | | |
| xxxx0010 | (3) | | | | | | | | | | | | | | | |
| xxxx0011 | (4) | | | | | | | | | | | | | | | |
| xxxx0100 | (5) | | | | | | | | | | | | | | | |
| xxxx0101 | (6) | | | | | | | | | | | | | | | |
| xxxx0110 | (7) | | | | | | | | | | | | | | | |
| xxxx0111 | (8) | | | | | | | | | | | | | | | |
| xxxx1000 | (1) | | | | | | | | | | | | | | | |
| xxxx1001 | (2) | | | | | | | | | | | | | | | |
| xxxx1010 | (3) | | | | | | | | | | | | | | | |
| xxxx1011 | (4) | | | | | | | | | | | | | | | |
| xxxx1100 | (5) | | | | | | | | | | | | | | | |
| xxxx1101 | (6) | | | | | | | | | | | | | | | |
| xxxx1110 | (7) | | | | | | | | | | | | | | | |
| xxxx1111 | (8) | | | | | | | | | | | | | | | |

Note: The user can specify any pattern for character-generator RAM.

**Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: A02)**

| Upper 4 Bits / Lower 4 Bits | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| xxxx0000 | CG RAM (1) |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0001 | (2) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0010 | (3) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0011 | (4) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0100 | (5) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0101 | (6) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0110 | (7) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx0111 | (8) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1000 | (1) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1001 | (2) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1010 | (3) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1011 | (4) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1100 | (5) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1101 | (6) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1110 | (7) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| xxxx1111 | (8) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)**

**For 5 × 8 dot character patterns**

| Character Codes (DDRAM data) 7 6 5 4 3 2 1 0 (High … Low) | CGRAM Address 5 4 3 2 1 0 (High … Low) | Character Patterns (CGRAM data) 7 6 5 4 3 2 1 0 (High … Low) | |
|---|---|---|---|
| 0 0 0 0 * 0 0 0 | 0 0 0 | * * * 1 1 1 1 0 | Character pattern (1) |
| | | * * * 1 0 0 0 1 | |
| | | * * * 1 0 0 0 1 | |
| | | * * * 1 1 1 1 0 | |
| | | * * * 1 0 1 0 0 | |
| | | * * * 1 0 0 1 0 | |
| | | * * * 1 0 0 0 1 | |
| | | * * * 0 0 0 0 0 | Cursor position |
| 0 0 0 0 * 0 0 1 | 0 0 1 | * * * 1 0 0 0 1 | Character pattern (2) |
| | | * * * 0 1 0 1 0 | |
| | | * * * 1 1 1 1 1 | |
| | | * * * 0 0 1 0 0 | |
| | | * * * 1 1 1 1 1 | |
| | | * * * 0 0 1 0 0 | |
| | | * * * 0 0 1 0 0 | |
| | | * * * 0 0 0 0 0 | Cursor position |
| | | * * * | |
| | | * * * | |
| 0 0 0 0 * 1 1 1 | 1 1 1 | | |
| | | * * * | |
| | | * * * | |
| | | * * * | |
| | | * * * | |

Notes: 1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).

2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor.

   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display.

   If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.

3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).

4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

**Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data) (cont)**

**For 5 × 10 dot character patterns**

| Character Codes (DDRAM data) | CGRAM Address | Character Patterns (CGRAM data) | |
|---|---|---|---|
| 7 6 5 4 3 2 1 0<br>High Low | 5 4 3 2 1 0<br>High Low | 7 6 5 4 3 2 1 0<br>High Low | |
| 0 0 0 0 * 0 0 * | 0 0 0 0 0 | * * * 0 0 0 0 0 | Character pattern |
| | 0 0 0 1 0 | * * * 0 0 0 0 0 | |
| | 0 0 1 0 0 | * * * 1 0 1 1 0 | |
| | 0 0 1 1 0 | * * * 1 1 0 0 1 | |
| | 0 1 0 0 0 | * * * 1 0 0 0 1 | |
| | 0 1 0 1 0 | * * * 1 0 0 0 1 | |
| | 0 1 1 0 0 | * * * 1 1 1 1 0 | |
| | 0 1 1 1 0 | * * * 1 0 0 0 0 | |
| | 1 0 0 0 0 | * * * 1 0 0 0 0 | |
| | 1 0 0 1 0 | * * * 1 0 0 0 0 | |
| | 1 0 1 0 0 | * * * 0 0 0 0 0 | Cursor position |
| | 1 0 1 1 0 | * * * * * * * * * | |
| | 1 1 0 0 0 | * * * * * * * * * | |
| | 1 1 0 1 0 | * * * * * * * * * | |
| | 1 1 1 0 0 | * * * * * * * * * | |
| | 1 1 1 1 0 | * * * * * * * * * | |
| 0 0 0 0 * 1 1 * | 0 0 0 0 0 | * * * | |
| | 0 0 0 1 0 | * * * | |
| | 1 0 0 1 0 | * * * | |
| | 1 0 1 0 0 | * * * | |
| | 1 0 1 1 0 | * * * * * * * * * | |
| | 1 1 0 0 0 | * * * * * * * * * | |
| | 1 1 0 1 0 | * * * * * * * * * | |
| | 1 1 1 0 0 | * * * * * * * * * | |
| | 1 1 1 1 0 | * * * * * * * * * | |

Notes: 1. Character code bits 1 and 2 correspond to CGRAM address bits 4 and 5 (2 bits: 4 types).

2. CGRAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.

   Maintain the 11th line data corresponding to the cursor display positon at 0 as the cursor display.

   If the 11th line data is “1”, “1” bits will light up the 11th line regardless of the cursor presence.

   Since lines 12 to 16 are not used for display, they can be used for general data RAM.

3. Character pattern row positions are the same as 5 × 8 dot character pattern positions.

4. CGRAM character patterns are selected when character code bits 4 to 7 are all 0.

   However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

* Indicates no effect.

### Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interferences, such as flickering, in areas other than the display area.

### Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When the character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output non-selection waveforms.

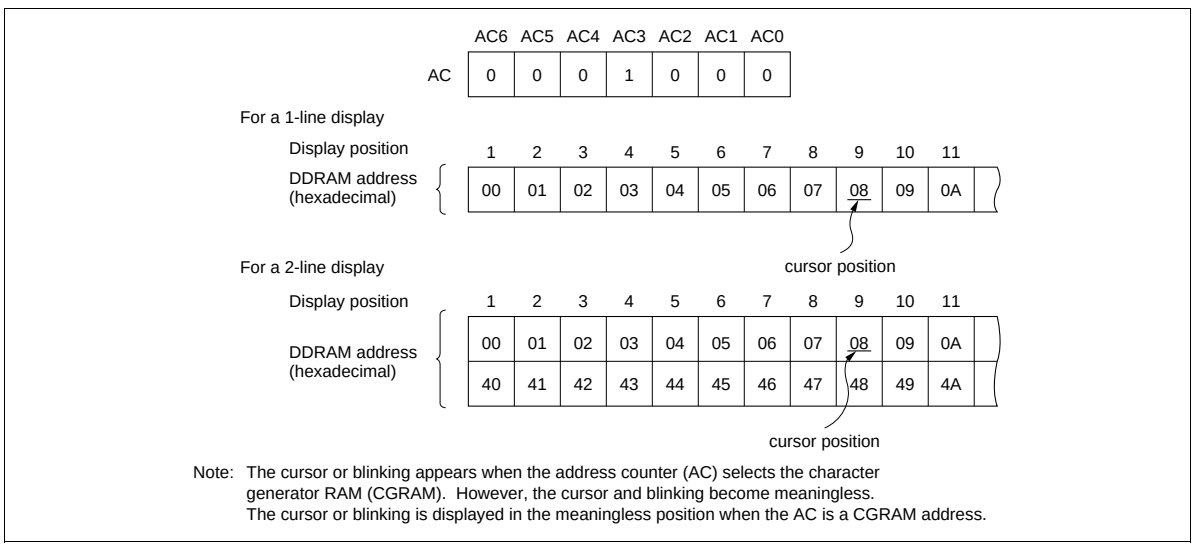
Sending serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DDRAM).

Since serial data is latched when the display data character pattern corresponding to the starting address enters the internal shift register, the HD44780U drives from the head display.

### Cursor/Blink Control Circuit

The cursor/blink control circuit generates the cursor or character blinking. The cursor or the blinking will appear with the digit located at the display data RAM (DDRAM) address set in the address counter (AC).

For example (Figure 8), when the address counter is 08H, the cursor position is displayed at DDRAM address 08H.




Note: The cursor or blinking appears when the address counter (AC) selects the character generator RAM (CGRAM). However, the cursor and blinking become meaningless. The cursor or blinking is displayed in the meaningless position when the AC is a CGRAM address.

**Figure 8 Cursor/Blink Display Example**

## Interfacing to the MPU

The HD44780U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

- For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the HD44780U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3).

  The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.
- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

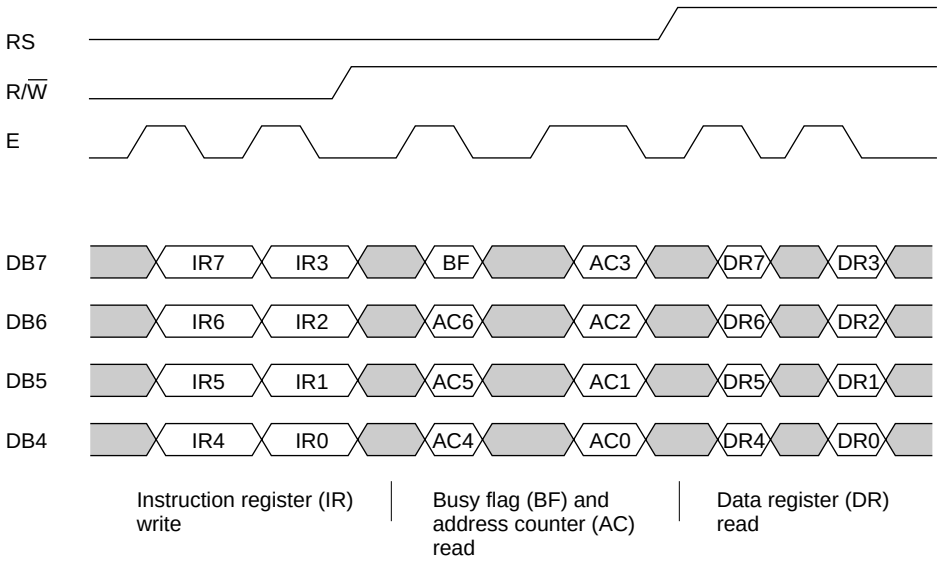



**Figure 9 4-Bit Transfer Example**

## Reset Function

### Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the HD44780U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after $V_{CC}$ rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 × 8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the HD44780U. For such a case, initial-ization must be performed by the MPU as explained in the section, Initializing by Instruction.

## Instructions

### Outline

Only the instruction register (IR) and the data register (DR) of the HD44780U can be controlled by the MPU. Before starting the internal operation of the HD44780U, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the HD44780U is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/

write signal (R/$\overline{W}$), and the data bus (DB0 to DB7), make up the HD44780U instructions (Table 6). There are four categories of instructions that:

- Designate HD44780U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD44780U RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (Table 11) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the HD44780U is not in the busy state (BF = 0) before sending an instruction from the MPU to the HD44780U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Table 6 for the list of each instruc-tion execution time.

**Table 6 Instructions**

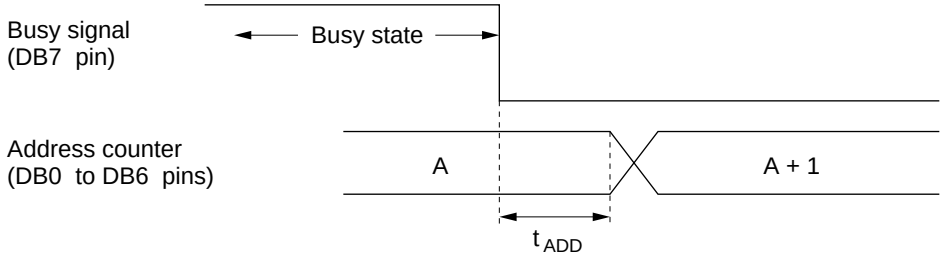
| | Code | | | | | | | | | | | Execution Time (max) (when $f_{cp}$ or $f_{osc}$ is 270 kHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Instruction** | **RS** | **R/$\overline{W}$** | **DB7** | **DB6** | **DB5** | **DB4** | **DB3** | **DB2** | **DB1** | **DB0** | **Description** | |
| Clear display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clears entire display and sets DDRAM address 0 in address counter. | |
| Return home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | — | Sets DDRAM address 0 in address counter. Also returns display from being shifted to original position. DDRAM contents remain unchanged. | 1.52 ms |
| Entry mode set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 37 µs |
| Display on/off control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B). | 37 µs |
| Cursor or display shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | — | — | Moves cursor and shifts display without changing DDRAM contents. | 37 µs |
| Function set | 0 | 0 | 0 | 0 | 1 | DL | N | F | — | — | Sets interface data length (DL), number of display lines (N), and character font (F). | 37 µs |
| Set CGRAM address | 0 | 0 | 0 | 1 | ACG | ACG | ACG | ACG | ACG | ACG | Sets CGRAM address. CGRAM data is sent and received after this setting. | 37 µs |
| Set DDRAM address | 0 | 0 | 1 | ADD | ADD | ADD | ADD | ADD | ADD | ADD | Sets DDRAM address. DDRAM data is sent and received after this setting. | 37 µs |
| Read busy flag & address | 0 | 1 | BF | AC | AC | AC | AC | AC | AC | AC | Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents. | 0 µs |

**Table 6 Instructions (cont)**

| Instruction | Code RS | R/$\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description | Execution Time (max) (when $f_{cp}$ or $f_{OSC}$ is 270 kHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write data to CG or DDRAM | 1 | 0 | Write data | | | | | | | | Writes data into DDRAM or CGRAM. | 37 µs<br>$t_{ADD}$ = 4 µs* |
| Read data from CG or DDRAM | 1 | 1 | Read data | | | | | | | | Reads data from DDRAM or CGRAM. | 37 µs<br>$t_{ADD}$ = 4 µs* |
| | I/D = 1: Increment<br>I/D = 0: Decrement<br>S = 1: Accompanies display shift<br>S/C = 1: Display shift<br>S/C = 0: Cursor move<br>R/L = 1: Shift to the right<br>R/L = 0: Shift to the left<br>DL = 1: 8 bits, DL = 0: 4 bits<br>N = 1: 2 lines, N = 0: 1 line<br>F = 1: 5 × 10 dots, F = 0: 5 × 8 dots<br>BF = 1: Internally operating<br>BF = 0: Instructions acceptable | | | | | | | | | | DDRAM: Display data RAM<br>CGRAM: Character generator RAM<br>ACG: CGRAM address<br>ADD: DDRAM address (corresponds to cursor address)<br>AC: Address counter used for both DD and CGRAM addresses | Execution time changes when frequency changes<br>Example:<br>When $f_{cp}$ or $f_{OSC}$ is 250 kHz,<br>$37\ \mu s \times \frac{270}{250} = 40\ \mu s$ |

Note: — indicates no effect.

* After execution of the CGRAM/DDRAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In Figure 10, $t_{ADD}$ is the time elapsed after the busy flag turns off until the address counter is updated.




Note: $t_{ADD}$ depends on the operation frequency
$t_{ADD}$ = 1.5/($f_{cp}$ or $f_{OSC}$) seconds

**Figure 10 Address Counter Update**

## Instruction Description

### Clear Display

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

### Return Home

Return home sets DDRAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DDRAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

### Entry Mode Set

**I/D:** Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CGRAM.

**S:** Shifts the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DDRAM. Also, writing into or reading out from CGRAM does not shift the display.

### Display On/Off Control

**D:** The display is on when D is 1 and off when D is 0. When off, the display data remains in DDRAM, but can be displayed instantly by setting D to 1.

**C:** The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 × 8 dot character font selection and in the 11th line for the 5 × 10 dot character font selection (Figure 13).

**B:** The character indicated by the cursor blinks when B is 1 (Figure 13). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when $f_{cp}$ or $f_{OSC}$ is 250 kHz. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to $f_{OSC}$ or the reciprocal of $f_{cp}$. For example, when $f_{cp}$ is 270 kHz, $409.6 \times 250/270 = 379.2$ ms.)

**Cursor or Display Shift**

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (Table 7). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

**Function Set**

**DL:** Sets the interface data length. Data is sent or received in 8-bit lengths (DB7 to DB0) when DL is 1, and in 4-bit lengths (DB7 to DB4) when DL is 0.When 4-bit length is selected, data must be sent or received twice.

**N:** Sets the number of display lines.

**F:** Sets the character font.

Note: Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

**Set CGRAM Address**

Set CGRAM address sets the CGRAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CGRAM.

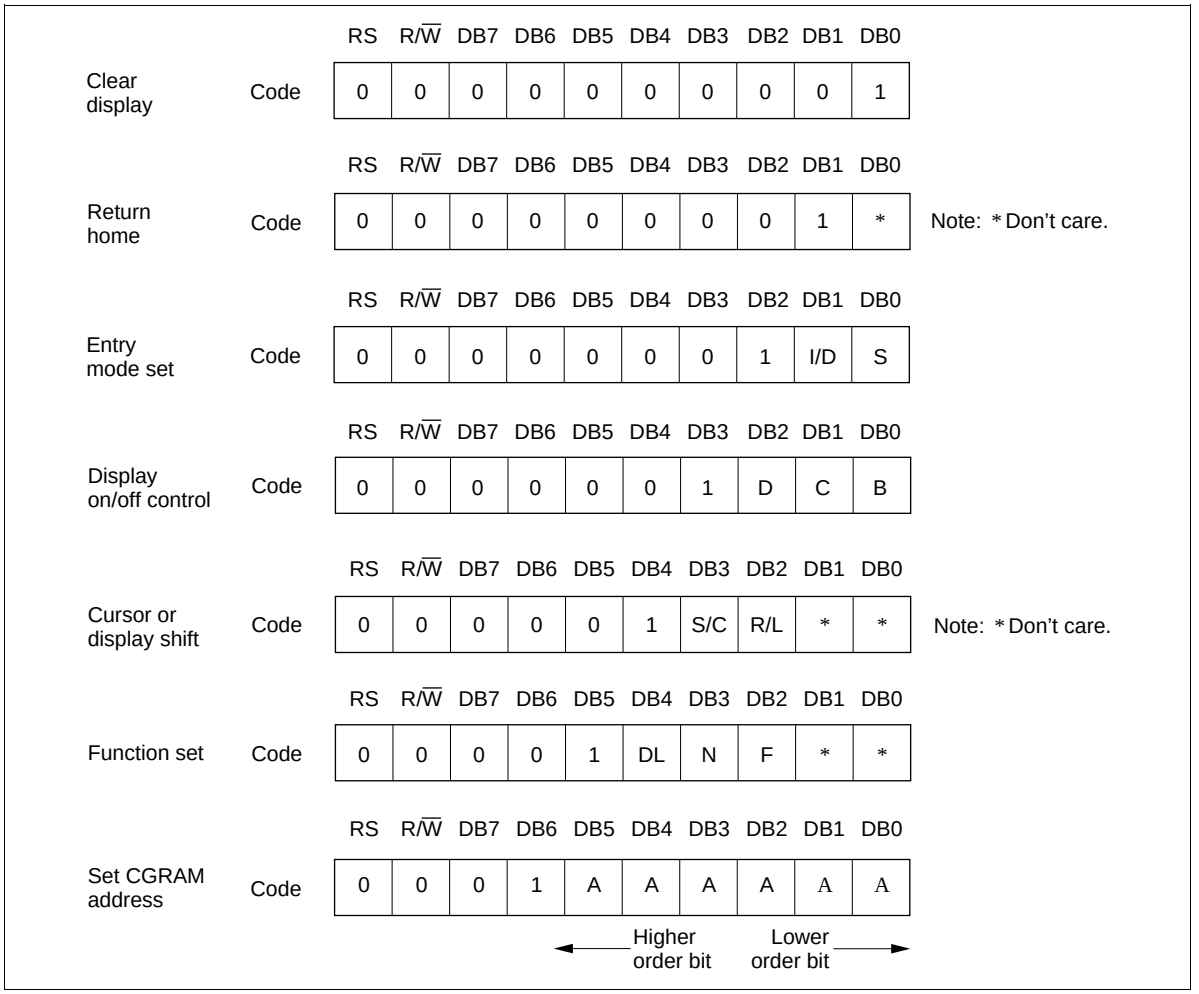



**Figure 11 Instruction (1)**

**Set DDRAM Address**

Set DDRAM address sets the DDRAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DDRAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

**Read Busy Flag and Address**

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out. This address counter is used by both CG and DDRAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CGRAM address and set DDRAM address.

**Table 7 Shift Function**

| S/C | R/L | |
|---|---|---|
| 0 | 0 | Shifts the cursor position to the left. (AC is decremented by one.) |
| 0 | 1 | Shifts the cursor position to the right. (AC is incremented by one.) |
| 1 | 0 | Shifts the entire display to the left. The cursor follows the display shift. |
| 1 | 1 | Shifts the entire display to the right. The cursor follows the display shift. |

**Table 8 Function Set**

| N | F | No. of Display Lines | Character Font | Duty Factor | Remarks |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 5 × 8 dots | 1/8 | |
| 0 | 1 | 1 | 5 × 10 dots | 1/11 | |
| 1 | * | 2 | 5 × 8 dots | 1/16 | Cannot display two lines for 5 × 10 dot character font |

Note: * Indicates don't care.

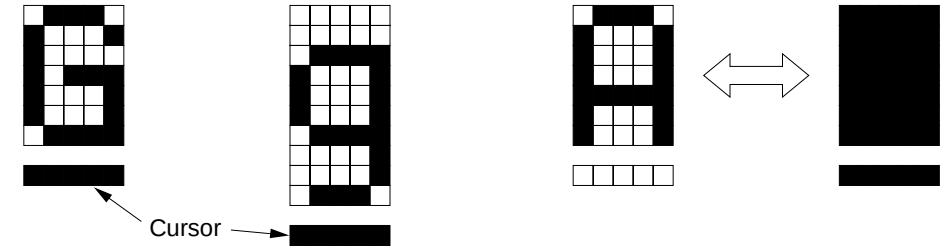



**Figure 12 Cursor and Blinking**

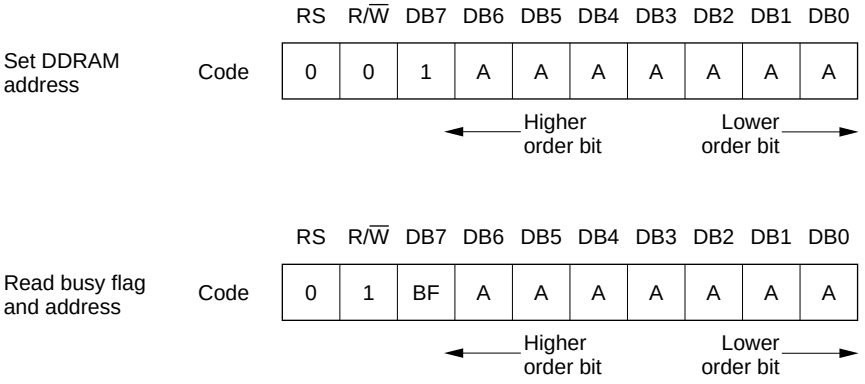



**Figure 13 Instruction (2)**

**Write Data to CG or DDRAM**

Write data to CG or DDRAM writes 8-bit binary data DDDDDDDD to CG or DDRAM.

To write into CG or DDRAM is determined by the previous specification of the CGRAM or DDRAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

**Read Data from CG or DDRAM**

Read data from CG or DDRAM reads 8-bit binary data DDDDDDDD from CG or DDRAM.

The previous designation determines whether CG or DDRAM is to be read. Before entering this read instruction, either CGRAM or DDRAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DDRAM). The operation of the cursor shift instruction is the same as the set DDRAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note: The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CGRAM or DDRAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DDRAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

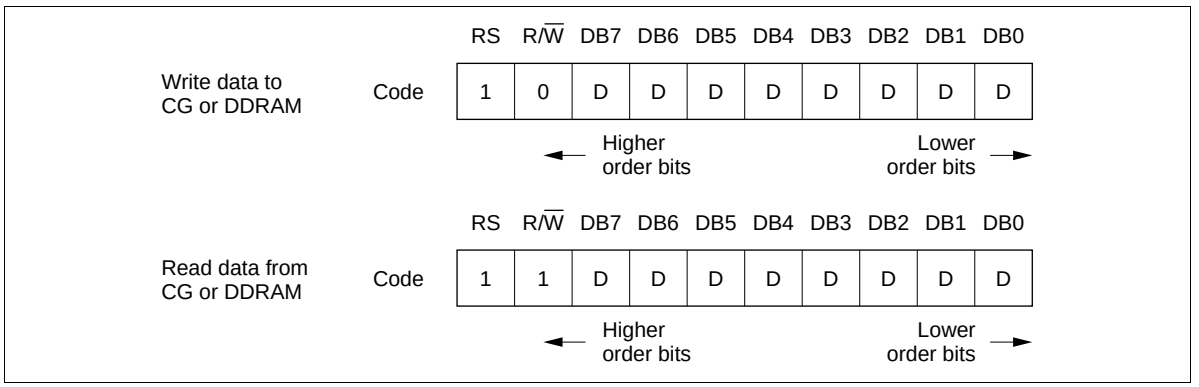



**Figure 14 Instruction (3)**

## Interfacing the HD44780U

### Interface to MPUs

- Interfacing to an 8-bit MPU

  See Figure 16 for an example of using a I/O port (for a single-chip microcomputer) as an interface device.

  In this example, P30 to P37 are connected to the data bus DB0 to DB7, and P75 to P77 are connected to E, R/$\overline{W}$, and RS, respectively.

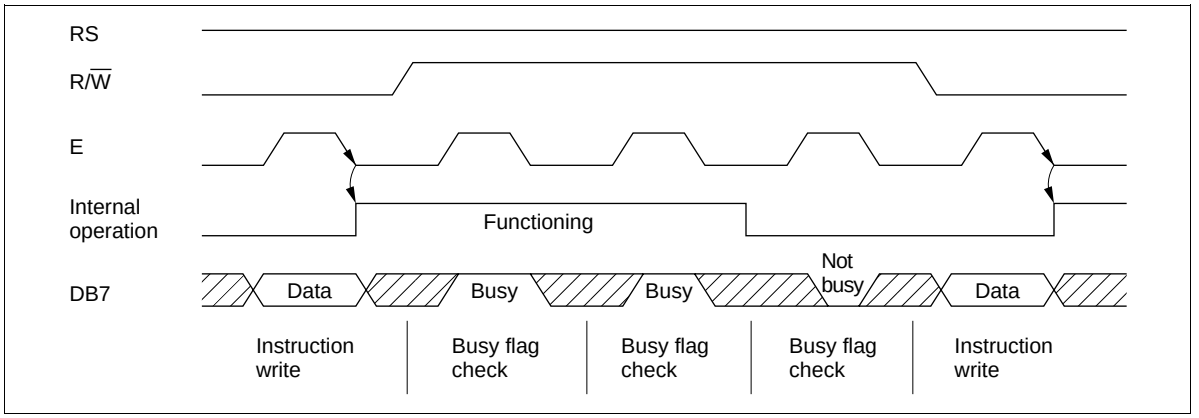



**Figure 15 Example of Busy Flag Check Timing Sequence**

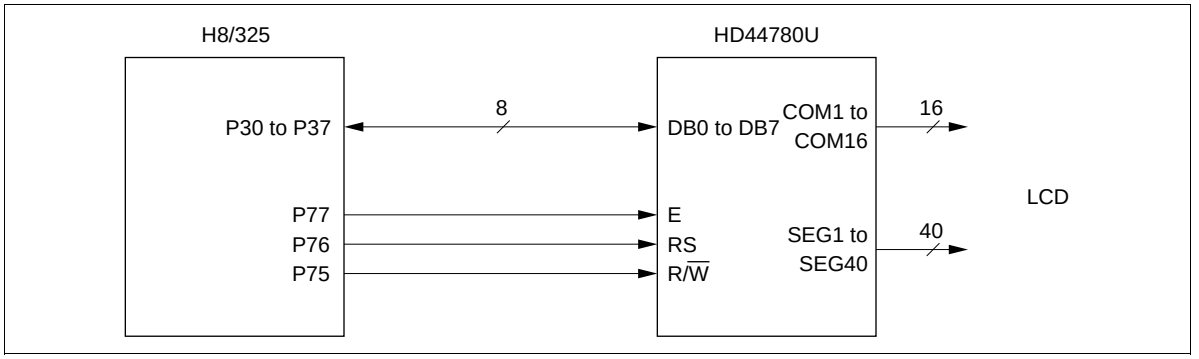


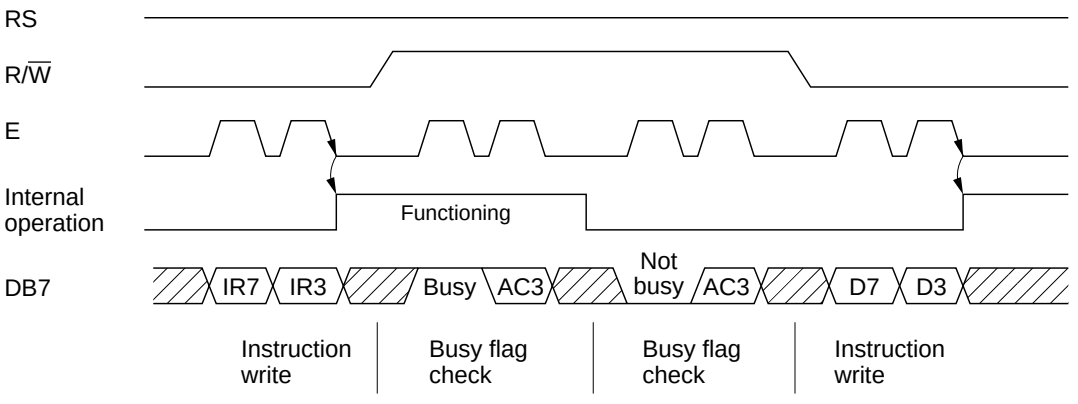

**Figure 16 H8/325 Interface (Single-Chip Mode)**

- Interfacing to a 4-bit MPU

  The HD44780U can be connected to the I/O port of a 4-bit MPU. If the I/O port has enough bits, 8-bit data can be transferred. Otherwise, one data transfer must be made in two operations for 4-bit data. In this case, the timing sequence becomes somewhat complex. (See Figure 17.)

  See Figure 18 for an interface example to the HMCS4019R.

  Note that two cycles are needed for the busy flag check as well as for the data transfer. The 4-bit operation is selected by the program.




Note: IR7 , IR3 are the 7th and 3rd bits of the instruction.
AC3 is the 3rd bit of the address counter.

**Figure 17 Example of 4-Bit Data Transfer Timing Sequence**

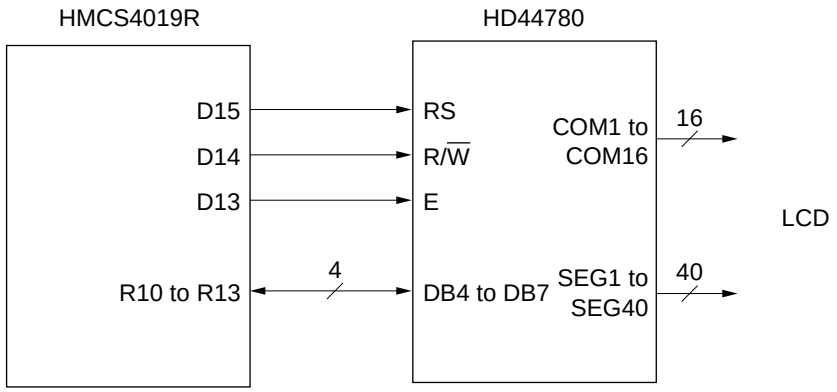



**Figure 18 Example of Interface to HMCS4019R**

### Interface to Liquid Crystal Display

**Character Font and Number of Lines:** The HD44780U can perform two types of displays, 5 × 8 dot and 5 × 10 dot character fonts, each with a cursor.

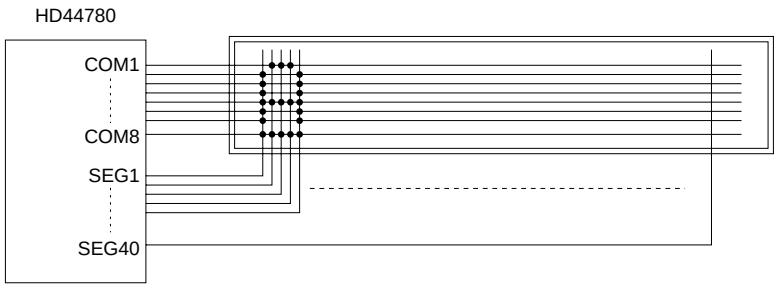
Up to two lines are displayed for 5 × 8 dots and one line for 5 × 10 dots. Therefore, a total of three types of common signals are available (Table 9).

The number of lines and font types can be selected by the program. (See Table 6, Instructions.)

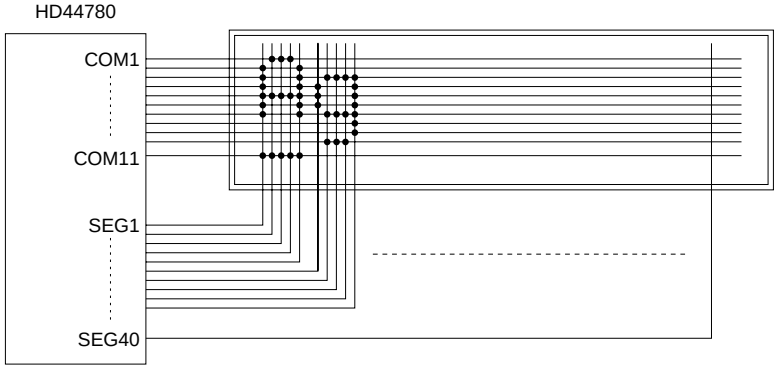
**Connection to HD44780 and Liquid Crystal Display:** See Figure 19 for the connection examples.

**Table 9 Common Signals**

| Number of Lines | Character Font | Number of Common Signals | Duty Factor |
|---|---|---|---|
| 1 | 5 × 8 dots + cursor | 8 | 1/8 |
| 1 | 5 × 10 dots + cursor | 11 | 1/11 |
| 2 | 5 × 8 dots + cursor | 16 | 1/16 |




Example of a 5 × 8 dot, 8-character × 1-line display (1/4 bias, 1/8 duty cycle)

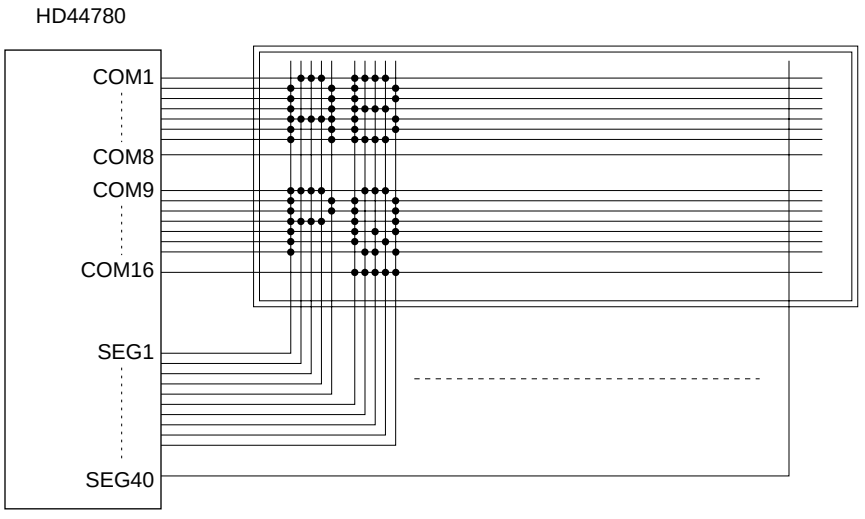



Example of a 5 × 10 dot, 8-character × 1-line display (1/4 bias, 1/11 duty cycle)

**Figure 19 Liquid Crystal Display and HD44780 Connections**

Since five segment signal lines can display one digit, one HD44780U can display up to 8 digits for a 1-line display and 16 digits for a 2-line display.

The examples in Figure 19 have unused common signal pins, which always output non-selection waveforms. When the liquid crystal display panel has unused extra scanning lines, connect the extra scanning lines to these common signal pins to avoid any undesirable effects due to crosstalk during the floating state.




Example of a 5 × 8 dot, 8-character × 2-line display (1/5 bias, 1/16 duty cycle)

**Figure 19 Liquid Crystal Display and HD44780 Connections (cont)**

**Connection of Changed Matrix Layout:** In the preceding examples, the number of lines correspond to the scanning lines. However, the following display examples (Figure 20) are made possible by altering the matrix layout of the liquid crystal display panel. In either case, the only change is the layout. The display characteristics and the number of liquid crystal display characters depend on the number of common signals or on duty factor. Note that the display data RAM (DDRAM) addresses for 4 characters × 2 lines and for 16 characters × 1 line are the same as in Figure 19.

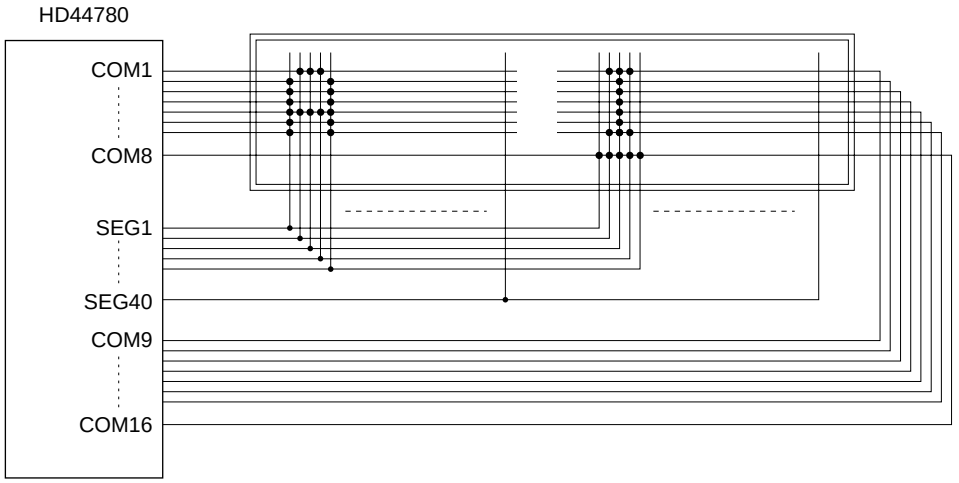



**Figure 20 Changed Matrix Layout Displays**

## Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to pins V1 to V5 of the HD44780U to obtain the liquid crystal display drive waveforms. The voltages must be changed according to the duty factor (Table 10).

VLCD is the peak value for the liquid crystal display drive waveforms, and resistance dividing provides voltages V1 to V5 (Figure 21).

**Table 10 Duty Factor and Power Supply for Liquid Crystal Display Drive**

| | Duty Factor | |
|---|---|---|
| | 1/8, 1/11 | 1/16 |
| | | Bias |
| Power Supply | 1/4 | 1/5 |
| V1 | $V_{cc}$–1/4 VLCD | $V_{cc}$–1/5 VLCD |
| V2 | $V_{cc}$–1/2 VLCD | $V_{cc}$–2/5 VLCD |
| V3 | $V_{cc}$–1/2 VLCD | $V_{cc}$–3/5 VLCD |
| V4 | $V_{cc}$–3/4 VLCD | $V_{cc}$–4/5 VLCD |
| V5 | $V_{cc}$–VLCD | $V_{cc}$–VLCD |

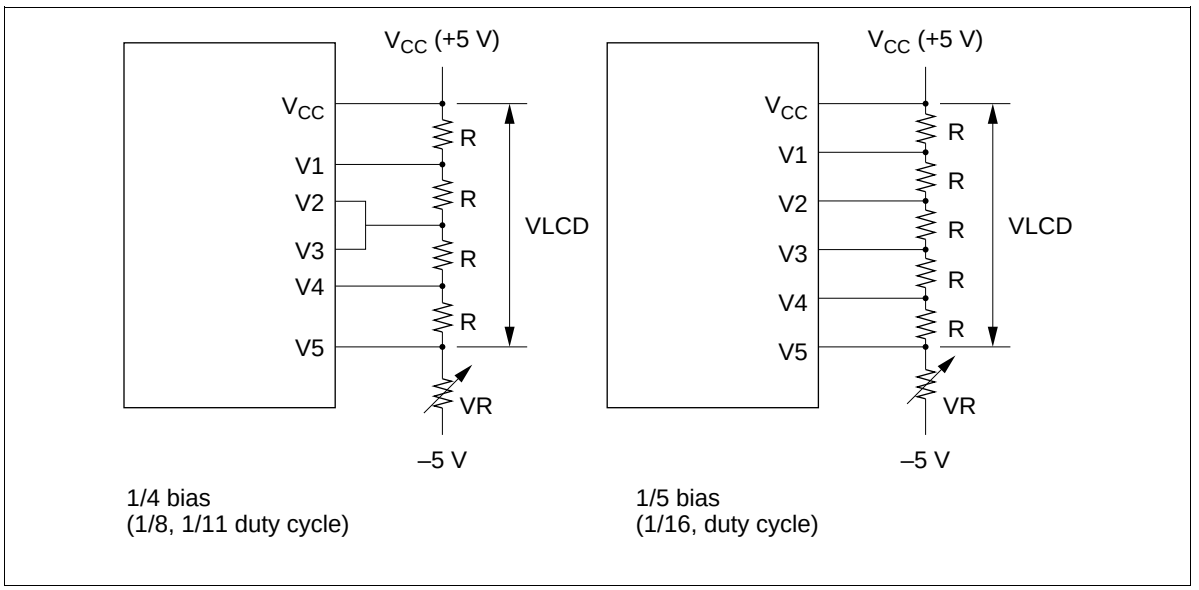



**Figure 21 Drive Voltage Supply Example**

## Relationship between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The liquid crystal display frame frequencies of Figure 22 apply only when the oscillation frequency is 270 kHz (one clock pulse of 3.7 μs).

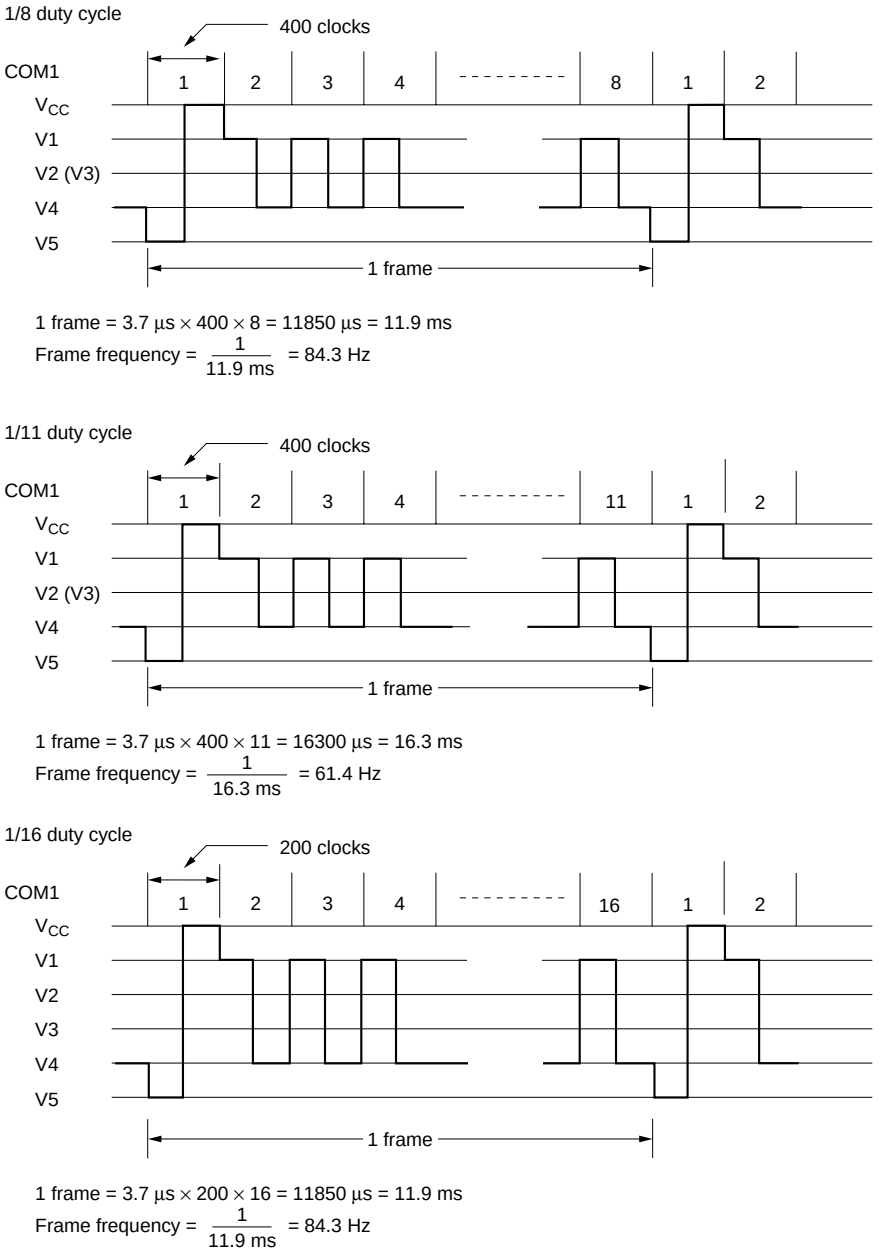



**Figure 22 Frame Frequency**

## Instruction and Display Correspondence

- 8-bit operation, 8-digit × 1-line display with internal reset

  Refer to Table 11 for an example of an 8-digit × 1-line display in 8-bit operation. The HD44780U functions must be set by the function set instruction prior to the display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays such as for advertising when combined with the display shift operation.

  Since the display shift operation changes only the display position with DDRAM contents unchanged, the first display data entered into DDRAM can be output when the return home operation is performed.

- 4-bit operation, 8-digit × 1-line display with internal reset

  The program must set all functions prior to the 4-bit operation (Table 12). When the power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since DB0 to DB3 are not connected, a rewrite is then required. However, since one operation is completed in two accesses for 4-bit operation, a rewrite is needed to set the functions (see Table 12). Thus, DB4 to DB7 of the function set instruction is written twice.

- 8-bit operation, 8-digit × 2-line display

  For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be again set after the 8th character is completed. (See Table 13.) Note that the display shift operation is performed for the first and second lines. In the example of Table 13, the display shift is performed when the cursor is on the second line. However, if the shift operation is performed when the cursor is on the first line, both the first and second lines move together. If the shift is repeated, the display of the second line will not move to the first line. The same display will only shift within its own line for the number of times the shift is repeated.

Note: When using the internal reset, the electrical characteristics in the Power Supply Conditions Using Internal Reset Circuit table must be satisfied. If not, the HD44780U must be initialized by instructions. See the section, Initializing by Instruction.

**Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset**

| Step No. | Instruction RS | R/$\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Display | Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Power supply on (the HD44780U is initialized by the internal reset circuit) | | | | | | | | | | | Initialized. No display. |
| 2 | Function set | | | | | | | | | | | Sets to 8-bit operation and selects 1-line display and 5 × 8 dot character font. (Number of display lines and character fonts cannot be changed after step #2.) |
| | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | * | * | | |
| 3 | Display on/off control | | | | | | | | | | | Turns on display and cursor. Entire display is in space mode because of initialization. |
| | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | _ | |
| 4 | Entry mode set | | | | | | | | | | | Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted. |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | _ | |
| 5 | Write data to CGRAM/DDRAM | | | | | | | | | | | Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | H_ | |
| 6 | Write data to CGRAM/DDRAM | | | | | | | | | | | Writes I. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | HI_ | |
| 7 | . | | | | . | | | | | | . | |
| | . | | | | . | | | | | | . | |
| | . | | | | . | | | | | | . | |
| | . | | | | . | | | | | | . | |
| | . | | | | . | | | | | | . | |
| 8 | Write data to CGRAM/DDRAM | | | | | | | | | | | Writes I. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | HITACHI_ | |
| 9 | Entry mode set | | | | | | | | | | | Sets mode to shift display at the time of write. |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | HITACHI_ | |
| 10 | Write data to CGRAM/DDRAM | | | | | | | | | | | Writes a space. |
| | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ITACHI _ | |

**Table 11 8-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset (cont)**

| Step | Instruction | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | RS | R/$\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Display | Operation |
| 11 | Write data to CGRAM/DDRAM | | | | | | | | | | TACHI M_ | Writes M. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | | |
| 12 | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| 13 | Write data to CGRAM/DDRAM | | | | | | | | | | MICROKO_ | Writes O. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | | |
| 14 | Cursor or display shift | | | | | | | | | | MICROKO | Shifts only the cursor position to the left. |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | * | * | | |
| 15 | Cursor or display shift | | | | | | | | | | MICROKO | Shifts only the cursor position to the left. |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | * | * | | |
| 16 | Write data to CGRAM/DDRAM | | | | | | | | | | ICROCO | Writes C over K.<br>The display moves to the left. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | | |
| 17 | Cursor or display shift | | | | | | | | | | MICROCO | Shifts the display and cursor position to the right. |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | * | * | | |
| 18 | Cursor or display shift | | | | | | | | | | MICROCO_ | Shifts the display and cursor position to the right. |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | * | * | | |
| 19 | Write data to CGRAM/DDRAM | | | | | | | | | | ICROCOM_ | Writes M. |
| | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | | |
| 20 | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| | | | | | | . | | | | | . | |
| 21 | Return home | | | | | | | | | | HITACHI | Returns both display and cursor to the original position (address 0). |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | |

**Table 12 4-Bit Operation, 8-Digit × 1-Line Display Example with Internal Reset**

| Step No. | Instruction RS | R/$\overline{W}$ | DB7 | DB6 | DB5 | DB4 | Display | Operation |
|---|---|---|---|---|---|---|---|---|
| 1 | Power supply on (the HD44780U is initialized by the internal reset circuit) | | | | | | | Initialized. No display. |
| 2 | Function set | | | | | | | Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write. |
| | 0 | 0 | 0 | 0 | 1 | 0 | | |
| 3 | Function set | | | | | | | Sets 4-bit operation and selects 1-line display and 5 × 8 dot character font. 4-bit operation starts from this step and resetting is necessary. (Number of display lines and character fonts cannot be changed after step #3.) |
| | 0 | 0 | 0 | 0 | 1 | 0 | | |
| | 0 | 0 | 0 | 0 | * | * | | |
| 4 | Display on/off control | | | | | | _ | Turns on display and cursor. Entire display is in space mode because of initialization. |
| | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | 0 | 0 | 1 | 1 | 1 | 0 | | |
| 5 | Entry mode set | | | | | | _ | Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted. |
| | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | 0 | 0 | 0 | 1 | 1 | 0 | | |
| 6 | Write data to CGRAM/DDRAM | | | | | | H_ | Writes H. The cursor is incremented by one and shifts to the right. |
| | 1 | 0 | 0 | 1 | 0 | 0 | | |
| | 1 | 0 | 1 | 0 | 0 | 0 | | |

Note: The control is the same as for 8-bit operation beyond step #6.

**Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset**

| Step No. | Instruction RS | R/$\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Display | Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Power supply on (the HD44780U is initialized by the internal reset circuit) | | | | | | | | | | | Initialized. No display. |
| 2 | Function set | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | * | * | Sets to 8-bit operation and selects 2-line display and 5 × 8 dot character font. |
| 3 | Display on/off control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Turns on display and cursor. All display is in space mode because of initialization. |
| 4 | Entry mode set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted. |
| 5 | Write data to CGRAM/DDRAM | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Writes H. DDRAM has already been selected by initialization when the power was turned on. The cursor is incremented by one and shifted to the right. |
| 6 | . . . . . | | | | | . | | | | | . . . . . | |
| 7 | Write data to CGRAM/DDRAM | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | Writes I. |
| 8 | Set DDRAM address | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Sets DDRAM address so that the cursor is positioned at the head of the second line. |

**Table 13 8-Bit Operation, 8-Digit × 2-Line Display Example with Internal Reset (cont)**

| Step No. | Instruction RS | R/$\overline{W}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Display | Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 9 | Write data to CGRAM/DDRAM 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | HITACHI<br>M_ | Writes M. |
| 10 | . | . | . | . | . | . | . | . | . | . | . | |
| 11 | Write data to CGRAM/DDRAM 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | HITACHI<br>MICROCO_ | Writes O. |
| 12 | Entry mode set 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | HITACHI<br>MICROCO_ | Sets mode to shift display at the time of write. |
| 13 | Write data to CGRAM/DDRAM 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | ITACHI<br>ICROCOM_ | Writes M. Display is shifted to the left. The first and second lines both shift at the same time. |
| 14 | . | . | . | . | . | . | . | . | . | . | . | |
| 15 | Return home 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | HITACHI<br>MICROCOM | Returns both display and cursor to the original position (address 0). |

## Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to Figures 23 and 24 for the procedures on 8-bit and 4-bit initializations, respectively.

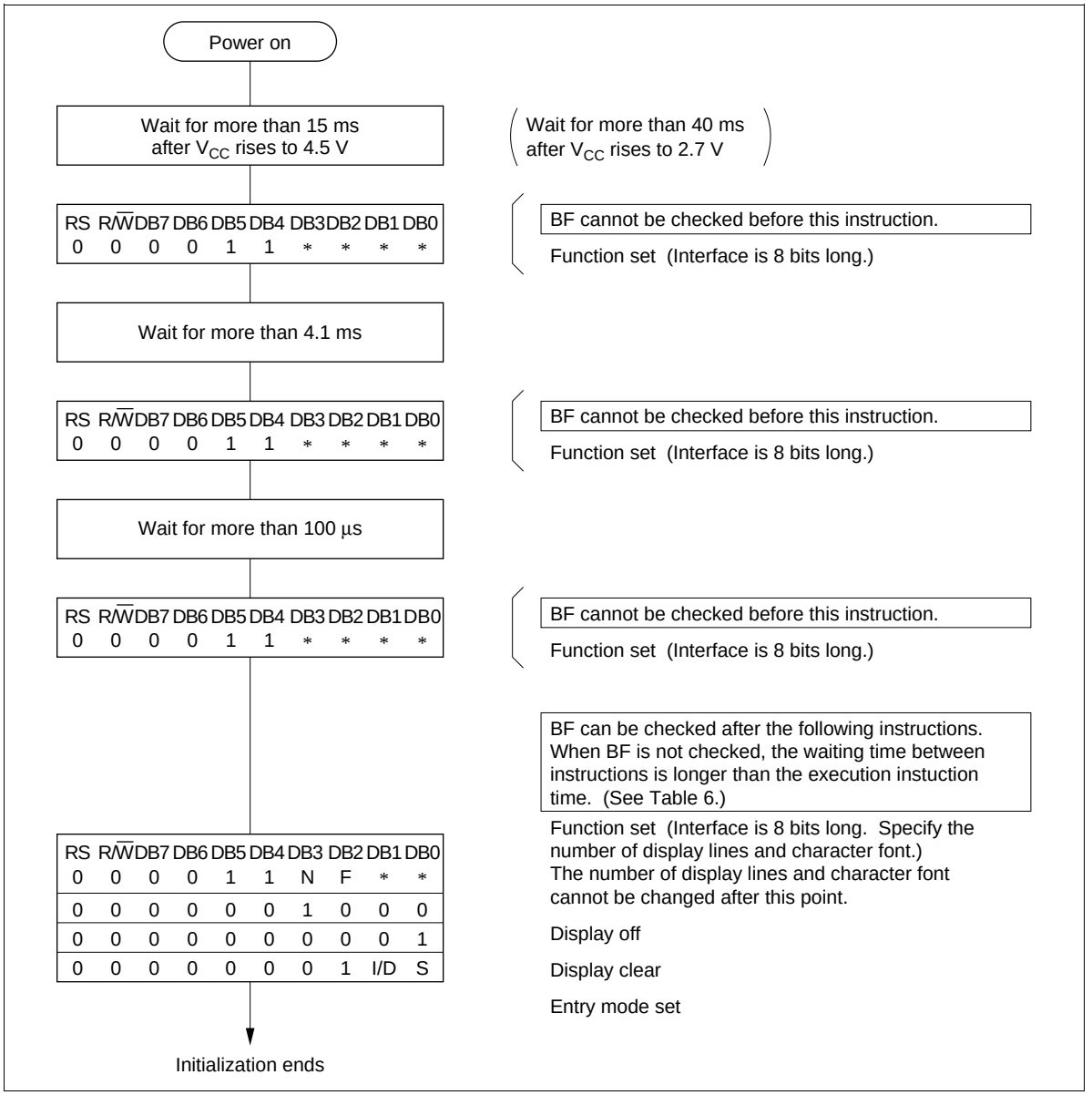



**Figure 23 8-Bit Interface**

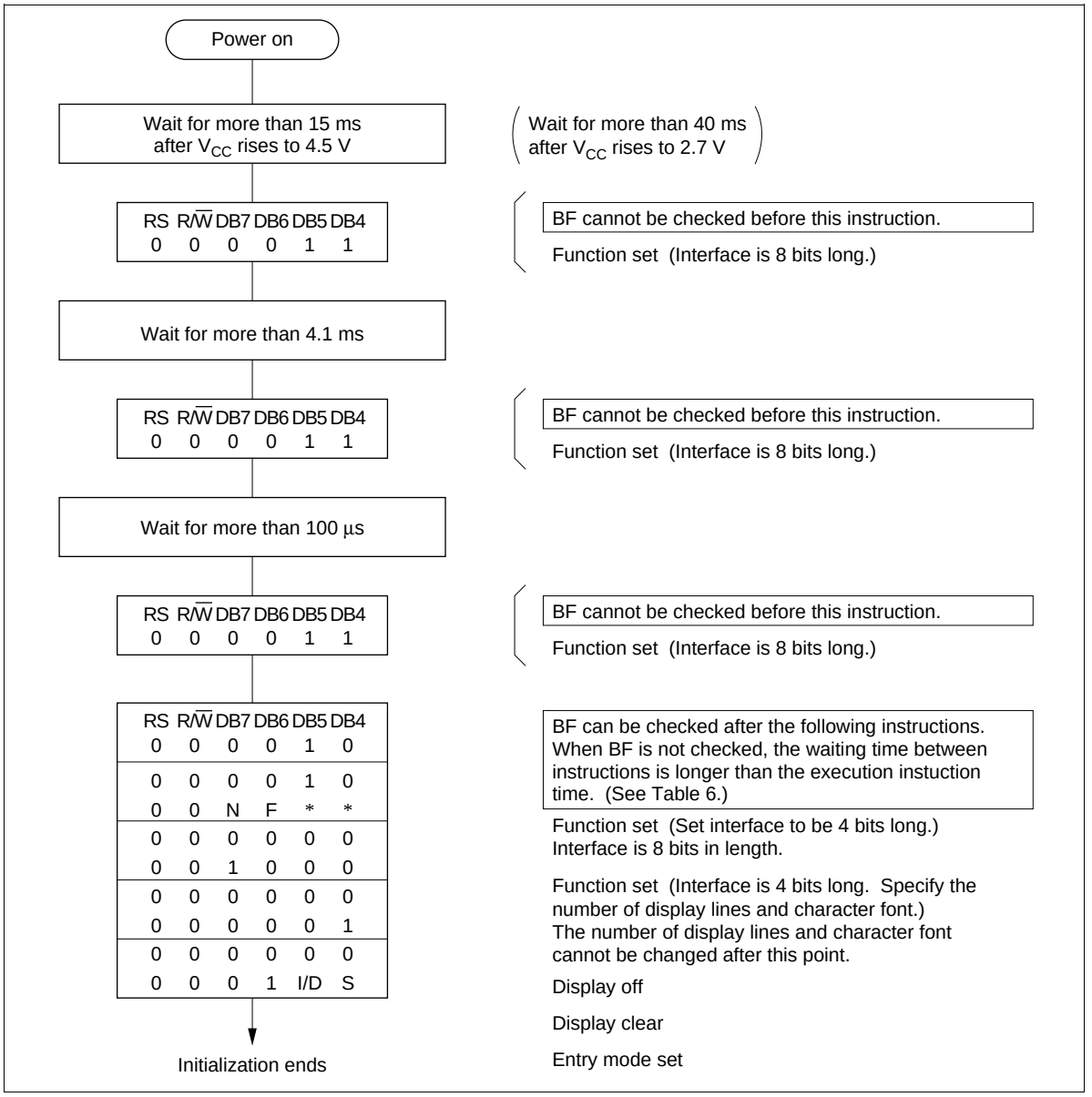



**Figure 24 4-Bit Interface**

## Absolute Maximum Ratings*

| Item | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Power supply voltage (1) | $V_{CC}$–GND | –0.3 to +7.0 | V | 1 |
| Power supply voltage (2) | $V_{CC}$–V5 | –0.3 to +13.0 | V | 1, 2 |
| Input voltage | Vt | –0.3 to $V_{CC}$ +0.3 | V | 1 |
| Operating temperature | $T_{opr}$ | –30 to +75 | °C | |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C | 4 |

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

## DC Characteristics ($V_{CC}$ = 2.7 to 4.5 V, $T_a$ = –30 to +75°C*[3])

| Item | Symbol | Min | Typ | Max | Unit | Test Condition | Notes* |
|---|---|---|---|---|---|---|---|
| Input high voltage (1) (except OSC1) | VIH1 | $0.7V_{CC}$ | — | $V_{CC}$ | V | | 6 |
| Input low voltage (1) (except OSC1) | VIL1 | –0.3 | — | 0.55 | V | | 6 |
| Input high voltage (2) (OSC1) | VIH2 | $0.7V_{CC}$ | — | $V_{CC}$ | V | | 15 |
| Input low voltage (2) (OSC1) | VIL2 | — | — | $0.2V_{CC}$ | V | | 15 |
| Output high voltage (1) (DB0–DB7) | VOH1 | $0.75V_{CC}$ | — | — | V | $–I_{OH}$ = 0.1 mA | 7 |
| Output low voltage (1) (DB0–DB7) | VOL1 | — | — | $0.2V_{CC}$ | V | $I_{OL}$ = 0.1 mA | 7 |
| Output high voltage (2) (except DB0–DB7) | VOH2 | $0.8V_{CC}$ | — | — | V | $–I_{OH}$ = 0.04 mA | 8 |
| Output low voltage (2) (except DB0–DB7) | VOL2 | — | — | $0.2V_{CC}$ | V | $I_{OL}$ = 0.04 mA | 8 |
| Driver on resistance (COM) | $R_{COM}$ | — | 2 | 20 | kΩ | ±Id = 0.05 mA, VLCD = 4 V | 13 |
| Driver on resistance (SEG) | $R_{SEG}$ | — | 2 | 30 | kΩ | ±Id = 0.05 mA, VLCD = 4 V | 13 |
| Input leakage current | $I_{LI}$ | –1 | — | 1 | µA | VIN = 0 to $V_{CC}$ | 9 |
| Pull-up MOS current (DB0–DB7, RS, R/$\overline{W}$) | $–I_p$ | 10 | 50 | 120 | µA | $V_{CC}$ = 3 V | |
| Power supply current | $I_{CC}$ | — | 150 | 300 | µA | $R_f$ oscillation, external clock $V_{CC}$ = 3 V, $f_{OSC}$ = 270 kHz | 10, 14 |
| LCD voltage | VLCD1 | 3.0 | — | 11.0 | V | $V_{CC}$–V5, 1/5 bias | 16 |
| | VLCD2 | 3.0 | — | 11.0 | V | $V_{CC}$–V5, 1/4 bias | 16 |

Note: * Refer to the Electrical Characteristics Notes section following these tables.

## AC Characteristics ($V_{CC}$ = 2.7 to 4.5 V, $T_a$ = –30 to +75°C*[3])

### Clock Characteristics

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition | Note* |
|---|---|---|---|---|---|---|---|---|
| External clock operation | External clock frequency | $f_{cp}$ | 125 | 250 | 350 | kHz | | 11 |
| | External clock duty | Duty | 45 | 50 | 55 | % | | |
| | External clock rise time | $t_{rcp}$ | — | — | 0.2 | µs | | |
| | External clock fall time | $t_{fcp}$ | — | — | 0.2 | µs | | |
| $R_f$ oscillation | Clock oscillation frequency | $f_{OSC}$ | 190 | 270 | 350 | kHz | $R_f$ = 75 kΩ, $V_{CC}$ = 3 V | 12 |

Note: * Refer to the Electrical Characteristics Notes section following these tables.

## Bus Timing Characteristics

### Write Operation

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Enable cycle time | $t_{cycE}$ | 1000 | — | — | ns | Figure 25 |
| Enable pulse width (high level) | $PW_{EH}$ | 450 | — | — | | |
| Enable rise/fall time | $t_{Er}$, $t_{Ef}$ | — | — | 25 | | |
| Address set-up time (RS, R/$\overline{W}$ to E) | $t_{AS}$ | 60 | — | — | | |
| Address hold time | $t_{AH}$ | 20 | — | — | | |
| Data set-up time | $t_{DSW}$ | 195 | — | — | | |
| Data hold time | $t_H$ | 10 | — | — | | |

### Read Operation

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Enable cycle time | $t_{cycE}$ | 1000 | — | — | ns | Figure 26 |
| Enable pulse width (high level) | $PW_{EH}$ | 450 | — | — | | |
| Enable rise/fall time | $t_{Er}$, $t_{Ef}$ | — | — | 25 | | |
| Address set-up time (RS, R/$\overline{W}$ to E) | $t_{AS}$ | 60 | — | — | | |
| Address hold time | $t_{AH}$ | 20 | — | — | | |
| Data delay time | $t_{DDR}$ | — | — | 360 | | |
| Data hold time | $t_{DHR}$ | 5 | — | — | | |

## Interface Timing Characteristics with External Driver

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| Clock pulse width | High level | $t_{CWH}$ | 800 | — | — | ns | Figure 27 |
| | Low level | $t_{CWL}$ | 800 | — | — | | |
| Clock set-up time | | $t_{CSU}$ | 500 | — | — | | |
| Data set-up time | | $t_{SU}$ | 300 | — | — | | |
| Data hold time | | $t_{DH}$ | 300 | — | — | | |
| M delay time | | $t_{DM}$ | –1000 | — | 1000 | | |
| Clock rise/fall time | | $t_{ct}$ | — | — | 200 | | |

## Power Supply Conditions Using Internal Reset Circuit

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Power supply rise time | $t_{rCC}$ | 0.1 | — | 10 | ms | Figure 28 |
| Power supply off time | $t_{OFF}$ | 1 | — | — | | |

## DC Characteristics ($V_{CC}$ = 4.5 to 5.5 V, $T_a$ = –30 to +75°C*[3])

| Item | Symbol | Min | Typ | Max | Unit | Test Condition | Notes* |
|---|---|---|---|---|---|---|---|
| Input high voltage (1) (except OSC1) | VIH1 | 2.2 | — | $V_{CC}$ | V | | 6 |
| Input low voltage (1) (except OSC1) | VIL1 | –0.3 | — | 0.6 | V | | 6 |
| Input high voltage (2) (OSC1) | VIH2 | $V_{CC}$–1.0 | — | $V_{CC}$ | V | | 15 |
| Input low voltage (2) (OSC1) | VIL2 | — | — | 1.0 | V | | 15 |
| Output high voltage (1) (DB0–DB7) | VOH1 | 2.4 | — | — | V | $–I_{OH}$ = 0.205 mA | 7 |
| Output low voltage (1) (DB0–DB7) | VOL1 | — | — | 0.4 | V | $I_{OL}$ = 1.2 mA | 7 |
| Output high voltage (2) (except DB0–DB7) | VOH2 | 0.9 $V_{CC}$ | — | — | V | $–I_{OH}$ = 0.04 mA | 8 |
| Output low voltage (2) (except DB0–DB7) | VOL2 | — | — | 0.1 $V_{CC}$ | V | $I_{OL}$ = 0.04 mA | 8 |
| Driver on resistance (COM) | RCOM | — | 2 | 20 | kΩ | ±Id = 0.05 mA, VLCD = 4 V | 13 |
| Driver on resistance (SEG) | RSEG | — | 2 | 30 | kΩ | ±Id = 0.05 mA, VLCD = 4 V | 13 |
| Input leakage current | $I_{LI}$ | –1 | — | 1 | µA | VIN = 0 to $V_{CC}$ | 9 |
| Pull-up MOS current (DB0–DB7, RS, R/$\overline{W}$) | $–I_p$ | 50 | 125 | 250 | µA | $V_{CC}$ = 5 V | |
| Power supply current | $I_{CC}$ | — | 350 | 600 | µA | $R_f$ oscillation, external clock $V_{CC}$ = 5 V, $f_{OSC}$ = 270 kHz | 10, 14 |
| LCD voltage | VLCD1 | 3.0 | — | 11.0 | V | $V_{CC}$–V5, 1/5 bias | 16 |
| | VLCD2 | 3.0 | — | 11.0 | V | $V_{CC}$–V5, 1/4 bias | 16 |

Note: * Refer to the Electrical Characteristics Notes section following these tables.

## AC Characteristics ($V_{CC}$ = 4.5 to 5.5 V, $T_a$ = –30 to +75°C*[3])

### Clock Characteristics

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition | Notes* |
|---|---|---|---|---|---|---|---|---|
| External clock operation | External clock frequency | $f_{cp}$ | 125 | 250 | 350 | kHz | | 11 |
| | External clock duty | Duty | 45 | 50 | 55 | % | | 11 |
| | External clock rise time | $t_{rcp}$ | — | — | 0.2 | µs | | 11 |
| | External clock fall time | $t_{fcp}$ | — | — | 0.2 | µs | | 11 |
| $R_f$ oscillation | Clock oscillation frequency | $f_{OSC}$ | 190 | 270 | 350 | kHz | $R_f$ = 91 kΩ<br>$V_{CC}$ = 5.0 V | 12 |

Note: * Refer to the Electrical Characteristics Notes section following these tables.

## Bus Timing Characteristics

### Write Operation

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Enable cycle time | $t_{cycE}$ | 500 | — | — | ns | Figure 25 |
| Enable pulse width (high level) | $PW_{EH}$ | 230 | — | — | | |
| Enable rise/fall time | $t_{Er}$, $t_{Ef}$ | — | — | 20 | | |
| Address set-up time (RS, R/$\overline{W}$ to E) | $t_{AS}$ | 40 | — | — | | |
| Address hold time | $t_{AH}$ | 10 | — | — | | |
| Data set-up time | $t_{DSW}$ | 80 | — | — | | |
| Data hold time | $t_H$ | 10 | — | — | | |

### Read Operation

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Enable cycle time | $t_{cycE}$ | 500 | — | — | ns | Figure 26 |
| Enable pulse width (high level) | $PW_{EH}$ | 230 | — | — | | |
| Enable rise/fall time | $t_{Er}$, $t_{Ef}$ | — | — | 20 | | |
| Address set-up time (RS, R/$\overline{W}$ to E) | $t_{AS}$ | 40 | — | — | | |
| Address hold time | $t_{AH}$ | 10 | — | — | | |
| Data delay time | $t_{DDR}$ | — | — | 160 | | |
| Data hold time | $t_{DHR}$ | 5 | — | — | | |

## Interface Timing Characteristics with External Driver

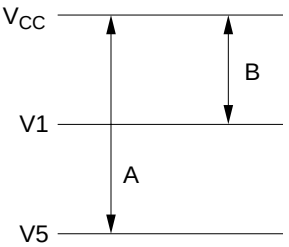
| Item | | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| Clock pulse width | High level | $t_{CWH}$ | 800 | — | — | ns | Figure 27 |
| | Low level | $t_{CWL}$ | 800 | — | — | | |
| Clock set-up time | | $t_{CSU}$ | 500 | — | — | | |
| Data set-up time | | $t_{SU}$ | 300 | — | — | | |
| Data hold time | | $t_{DH}$ | 300 | — | — | | |
| M delay time | | $t_{DM}$ | –1000 | — | 1000 | | |
| Clock rise/fall time | | $t_{ct}$ | — | — | 100 | | |

## Power Supply Conditions Using Internal Reset Circuit

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Power supply rise time | $t_{rCC}$ | 0.1 | — | 10 | ms | Figure 28 |
| Power supply off time | $t_{OFF}$ | 1 | — | — | | |

## Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V.

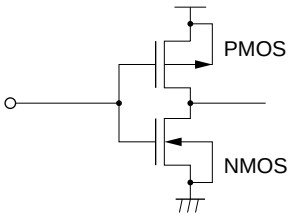



$A = V_{CC} - V5$
$B = V_{CC} - V1$
$A \geq 1.5$ V
$B \leq 0.25 \times A$

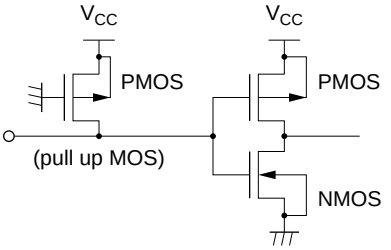
The conditions of V1 and V5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified as LCD voltage VLCD.

2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained.
3. For die products, specified at 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

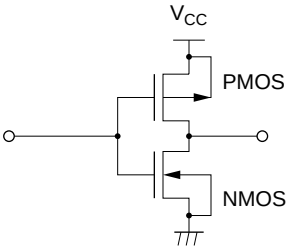
Input pin
Pin: E (MOS without pull-up)



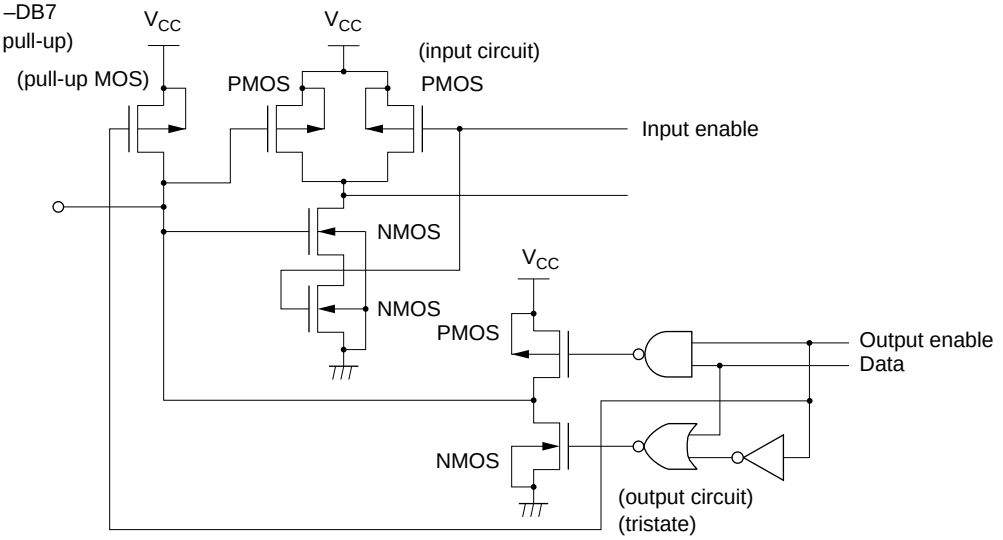

Pins: RS, R/$\overline{W}$ (MOS with pull-up)



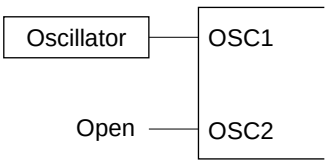

Output pin
Pins: CL1, CL2, M, D

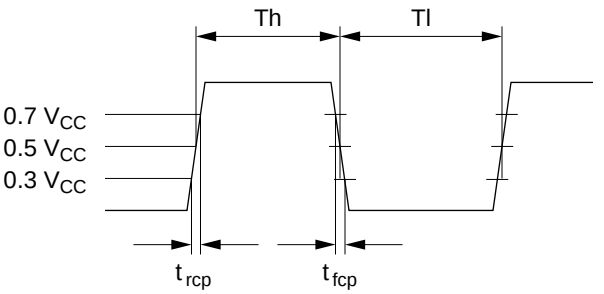



I/O Pin
Pins: DB0 –DB7
(MOS with pull-up)



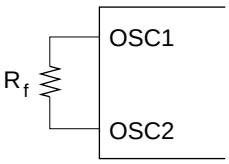
6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull–up MOSs, excluding output drive MOSs.
10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.
11. Applies only to external clock operation.



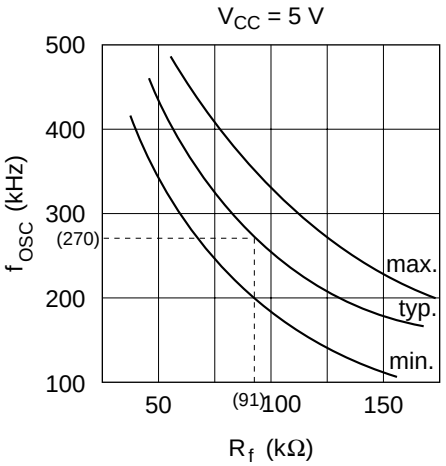



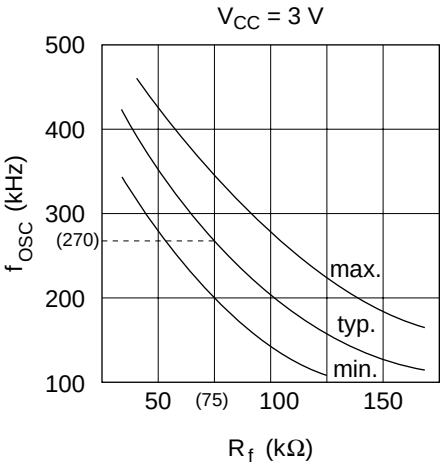

$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

12. Applies only to the internal oscillator operation using oscillation resistor $R_f$.




$R_f$: 75 kΩ ± 2% (when $V_{CC}$ = 3 V)
$R_f$: 91 kΩ ± 2% (when $V_{CC}$ = 5 V)
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

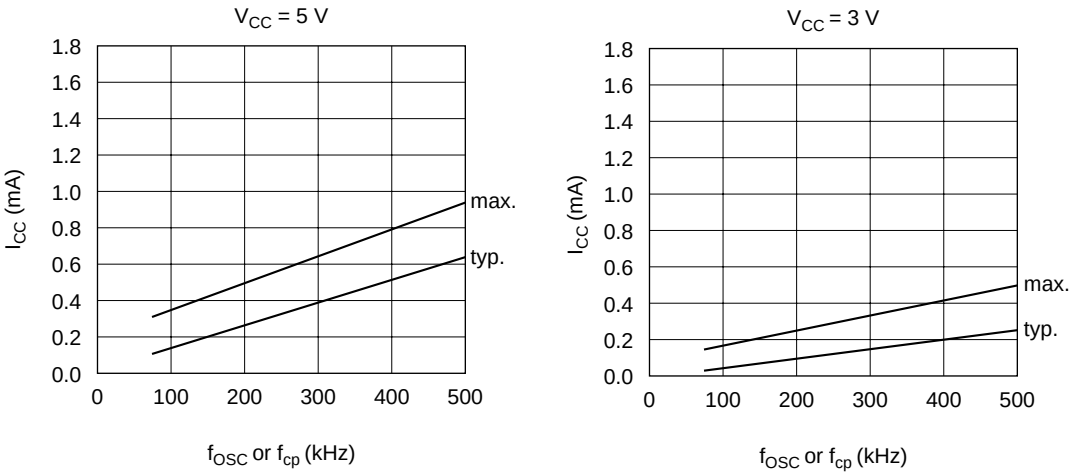


13. RCOM is the resistance between the power supply pins ($V_{CC}$, V1, V4, V5) and each common signal pin (COM1 to COM16).

    RSEG is the resistance between the power supply pins ($V_{CC}$, V2, V3, V5) and each segment signal pin (SEG1 to SEG40).

14. The following graphs show the relationship between operation frequency and current consumption.

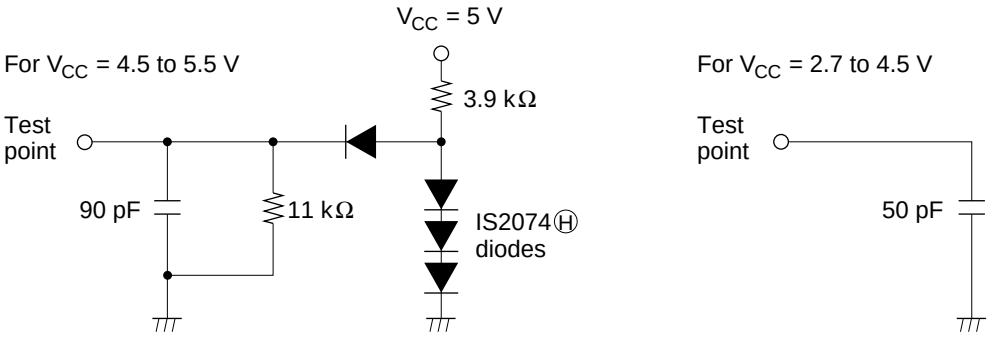



15. Applies to the OSC1 pin.

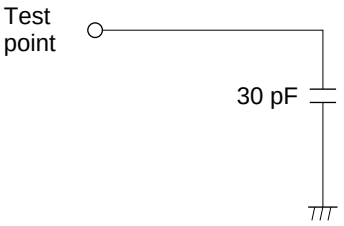
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage ($V_{CC}$, V1, V2, V3, V4, V5) when there is no load.

## Load Circuits

### Data Bus DB0 to DB7




### External Driver Control Signals: CL1, CL2, D, M



## Timing Characteristics

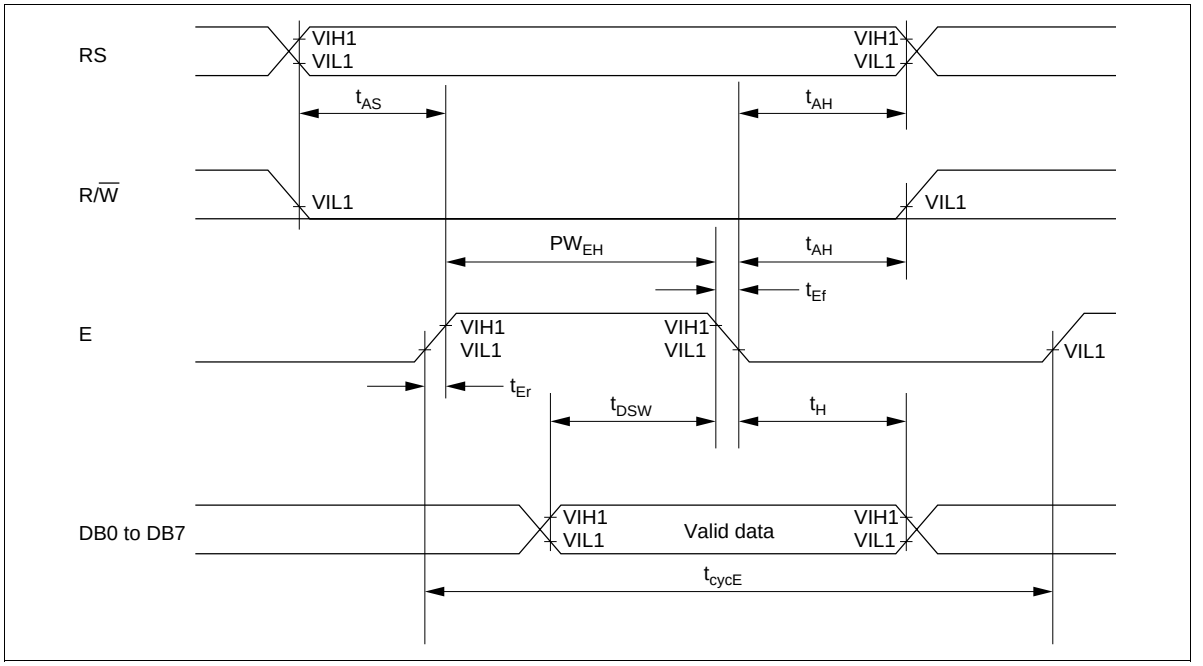
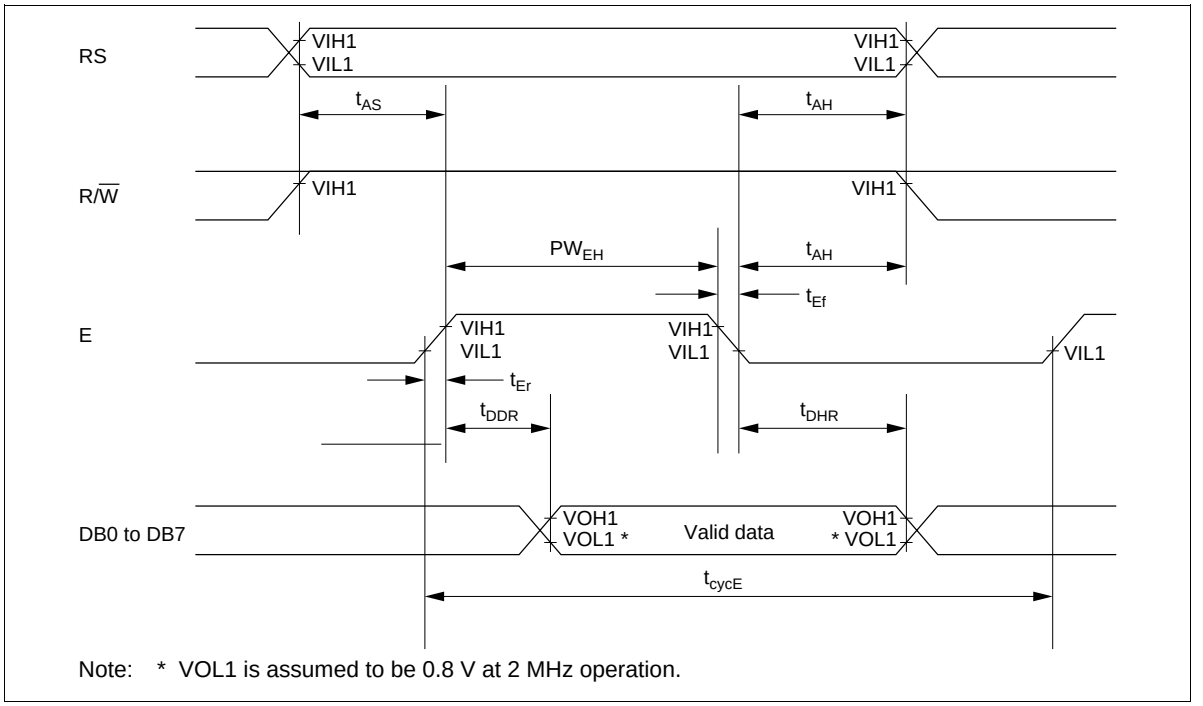



**Figure 25 Write Operation**




Note: * VOL1 is assumed to be 0.8 V at 2 MHz operation.

**Figure 26 Read Operation**

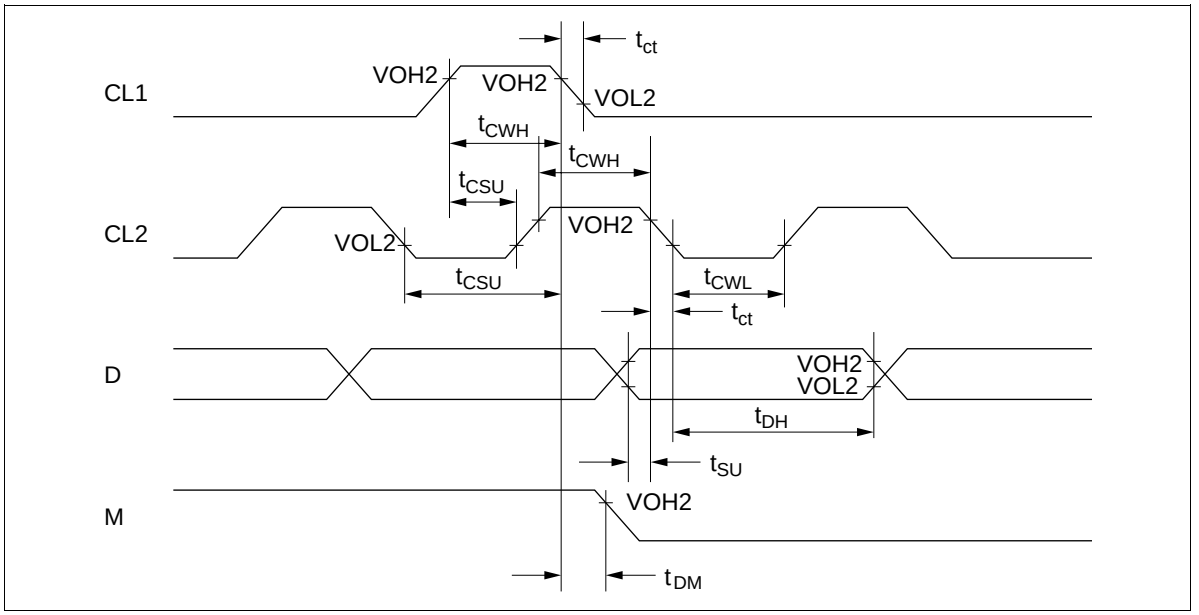
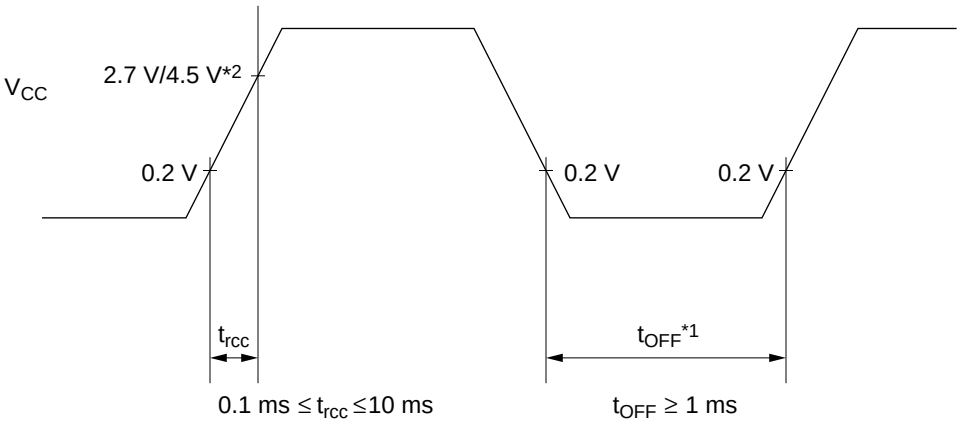



**Figure 27 Interface Timing with External Driver**




Notes: 1. $t_{OFF}$ compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-V operation, and at 2.7 V for 3-V operation.
3. For if 4.5 V is not reached during 5-V operation, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software. (Refer to the Initializing by Instruction section.)

**Figure 28 Internal Power Supply Reset**

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FAIRCHILD
SEMICONDUCTOR®

# KBL005 - KBL10


### Features

- Ideal for printed circuit board .
- Reliable low cost construction.
- High surge current capability.
- UL certified, UL #E96005.

## Bridge Rectifiers

### Absolute Maximum Ratings*

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Value | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | 005 | 01 | 02 | 04 | 06 | 08 | 10 | |
| $V_{RRM}$ | Maximum Repetitive Reverse Voltage | 50 | 100 | 200 | 400 | 600 | 800 | 1000 | V |
| $V_{RMS}$ | Maximum RMS Bridge Input Voltage | 35 | 70 | 140 | 280 | 420 | 560 | 700 | V |
| $V_R$ | DC Reverse Voltage (Rated $V_R$) | 50 | 100 | 200 | 400 | 600 | 800 | 1000 | V |
| $I_{F(AV)}$ | Average Rectified Forward Current, @ $T_A$ = 50°C | 4.0 | | | | | | | A |
| $I_{FSM}$ | Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave | 200 | | | | | | | A |
| $T_{stg}$ | Storage Temperature Range | -55 to +150 | | | | | | | °C |
| $T_J$ | Operating Junction Temperature | -55 to +150 | | | | | | | °C |

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

### Thermal Characteristics

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $P_D$ | Power Dissipation | 6.58 | W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient,* per leg | 19 | °C/W |
| $R_{\theta JL}$ | Thermal Resistance, Junction to Lead,* per leg | 2.4 | °C/W |

*Device mounted on PCB with 0.375 " (9.5 mm) lead length and 0.5 x 0.5" (13 x 13 mm) copper pads.

### Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Device | Units |
|---|---|---|---|
| $V_F$ | Forward Voltage, per bridge @ 4.0 A | 1.1 | V |
| $I_R$ | Reverse Current, total bridge @ rated $V_R$<br>$T_A$ = 25°C<br>$T_A$ = 100°C | <br>5.0<br>500 | <br>µA<br>µA |

## Typical Characteristics

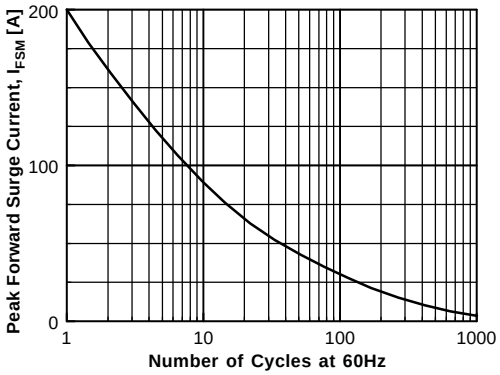


**Figure 1. Non-Repetitive Surge Current**

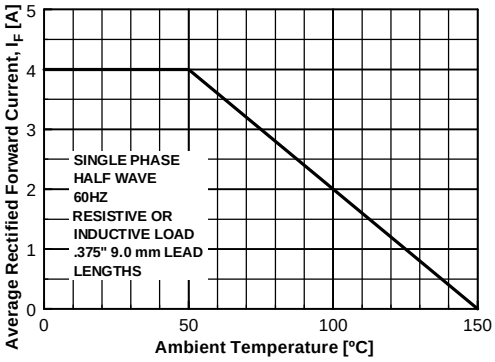


**Figure 2. Forward Current Derating Curve**

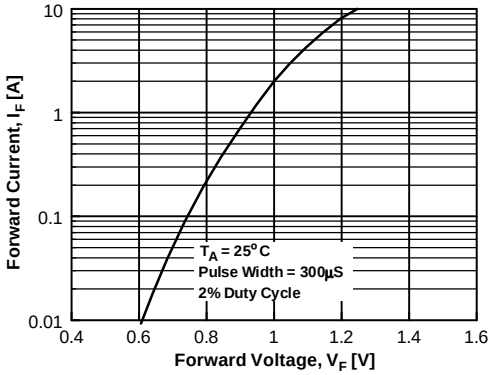


**Figure 3. Forward Voltage Characteristics**

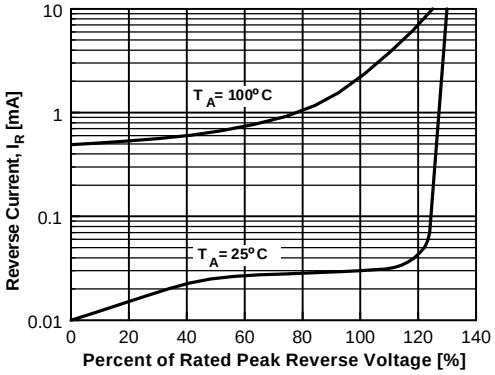


**Figure 4. Reverse Current vs Reverse Voltage**

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**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

19-0122; Rev 8; 10/03

MAXIM

# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers



## General Description

The MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The MAX483, MAX487, MAX488, and MAX489 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481, MAX485, MAX490, MAX491, and MAX1487 are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw between 120µA and 500µA of supply current when unloaded or fully loaded with disabled drivers. Additionally, the MAX481, MAX483, and MAX487 have a low-current shutdown mode in which they consume only 0.1µA. All parts operate from a single 5V supply.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487 and MAX1487 feature quarter-unit-load receiver input impedance, allowing up to 128 MAX487/MAX1487 transceivers on the bus. Full-duplex communications are obtained using the MAX488–MAX491, while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are designed for half-duplex applications.

## Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

## Next Generation Device Features

- **For Fault-Tolerant Applications**
  **MAX3430: ±80V Fault-Protected, Fail-Safe, 1/4 Unit Load, +3.3V, RS-485 Transceiver**
  **MAX3440E–MAX3444E: ±15kV ESD-Protected, ±60V Fault-Protected, 10Mbps, Fail-Safe, RS-485/J1708 Transceivers**
- **For Space-Constrained Applications**
  **MAX3460–MAX3464: +5V, Fail-Safe, 20Mbps, Profibus RS-485/RS-422 Transceivers**
  **MAX3362: +3.3V, High-Speed, RS-485/RS-422 Transceiver in a SOT23 Package**
  **MAX3280E–MAX3284E: ±15kV ESD-Protected, 52Mbps, +3V to +5.5V, SOT23, RS-485/RS-422, True Fail-Safe Receivers**
  **MAX3293/MAX3294/MAX3295: 20Mbps, +3.3V, SOT23, RS-855/RS-422 Transmitters**
- **For Multiple Transceiver Applications**
  **MAX3030E–MAX3033E: ±15kV ESD-Protected, +3.3V, Quad RS-422 Transmitters**
- **For Fail-Safe Applications**
  **MAX3080–MAX3089: Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceivers**
- **For Low-Voltage Applications**
  **MAX3483E/MAX3485E/MAX3486E/MAX3488E/MAX3490E/MAX3491E: +3.3V Powered, ±15kV ESD-Protected, 12Mbps, Slew-Rate-Limited, True RS-485/RS-422 Transceivers**

***Ordering Information appears at end of data sheet.***

## Selection Table

| PART NUMBER | HALF/FULL DUPLEX | DATA RATE (Mbps) | SLEW-RATE LIMITED | LOW-POWER SHUTDOWN | RECEIVER/ DRIVER ENABLE | QUIESCENT CURRENT (µA) | NUMBER OF TRANSMITTERS ON BUS | PIN COUNT |
|---|---|---|---|---|---|---|---|---|
| **MAX481** | Half | 2.5 | No | Yes | Yes | 300 | 32 | 8 |
| **MAX483** | Half | 0.25 | Yes | Yes | Yes | 120 | 32 | 8 |
| **MAX485** | Half | 2.5 | No | No | Yes | 300 | 32 | 8 |
| **MAX487** | Half | 0.25 | Yes | Yes | Yes | 120 | 128 | 8 |
| **MAX488** | Full | 0.25 | Yes | No | No | 120 | 32 | 8 |
| **MAX489** | Full | 0.25 | Yes | No | Yes | 120 | 32 | 14 |
| **MAX490** | Full | 2.5 | No | No | No | 300 | 32 | 8 |
| **MAX491** | Full | 2.5 | No | No | Yes | 300 | 32 | 14 |
| **MAX1487** | Half | 2.5 | No | No | Yes | 230 | 128 | 8 |

# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC}$) ..... 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to ($V_{CC}$ + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to ($V_{CC}$ + 0.5V)
Driver Output Voltage (A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to ($V_{CC}$ +0.5V)
Continuous Power Dissipation ($T_A$ = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ....727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) ..... 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) ..... 667mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) ..... 830mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) ..... 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) ..... 727mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487C_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487E_ A ..... -40°C to +85°C
MAX4_ _MJ_/MAX1487MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Differential Driver Output (no load) | $V_{OD1}$ | | | | | 5 | V |
| Differential Driver Output (with load) | $V_{OD2}$ | R = 50Ω (RS-422) | | 2 | | | V |
| | | R = 27Ω (RS-485), Figure 4 | | 1.5 | | 5 | |
| Change in Magnitude of Driver Differential Output Voltage for Complementary Output States | $\Delta V_{OD}$ | R = 27Ω or 50Ω, Figure 4 | | | | 0.2 | V |
| Driver Common-Mode Output Voltage | $V_{OC}$ | R = 27Ω or 50Ω, Figure 4 | | | | 3 | V |
| Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States | $\Delta V_{OD}$ | R = 27Ω or 50Ω, Figure 4 | | | | 0.2 | V |
| Input High Voltage | $V_{IH}$ | DE, DI, $\overline{RE}$ | | 2.0 | | | V |
| Input Low Voltage | $V_{IL}$ | DE, DI, $\overline{RE}$ | | | | 0.8 | V |
| Input Current | $I_{IN1}$ | DE, DI, $\overline{RE}$ | | | | ±2 | µA |
| Input Current (A, B) | $I_{IN2}$ | DE = 0V; $V_{CC}$ = 0V or 5.25V, all devices except MAX487/MAX1487 | $V_{IN}$ = 12V | | | 1.0 | mA |
| | | | $V_{IN}$ = -7V | | | -0.8 | |
| | | MAX487/MAX1487, DE = 0V, $V_{CC}$ = 0V or 5.25V | $V_{IN}$ = 12V | | | 0.25 | mA |
| | | | $V_{IN}$ = -7V | | | -0.2 | |
| Receiver Differential Threshold Voltage | $V_{TH}$ | -7V ≤ $V_{CM}$ ≤ 12V | | -0.2 | | 0.2 | V |
| Receiver Input Hysteresis | $\Delta V_{TH}$ | $V_{CM}$ = 0V | | | 70 | | mV |
| Receiver Output High Voltage | $V_{OH}$ | $I_O$ = -4mA, $V_{ID}$ = 200mV | | 3.5 | | | V |
| Receiver Output Low Voltage | $V_{OL}$ | $I_O$ = 4mA, $V_{ID}$ = -200mV | | | | 0.4 | V |
| Three-State (high impedance) Output Current at Receiver | $I_{OZR}$ | 0.4V ≤ $V_O$ ≤ 2.4V | | | | ±1 | µA |
| Receiver Input Resistance | $R_{IN}$ | -7V ≤ $V_{CM}$ ≤ 12V, all devices except MAX487/MAX1487 | | 12 | | | kΩ |
| | | -7V ≤ $V_{CM}$ ≤ 12V, MAX487/MAX1487 | | 48 | | | kΩ |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ = 5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| No-Load Supply Current (Note 3) | $I_{CC}$ | MAX488/MAX489, DE, DI, $\overline{RE}$ = 0V or $V_{CC}$ | | | | 120 | 250 | µA |
| | | MAX490/MAX491, DE, DI, $\overline{RE}$ = 0V or $V_{CC}$ | | | | 300 | 500 | |
| | | MAX481/MAX485, $\overline{RE}$ = 0V or $V_{CC}$ | DE = $V_{CC}$ | | | 500 | 900 | |
| | | | DE = 0V | | | 300 | 500 | |
| | | MAX1487, $\overline{RE}$ = 0V or $V_{CC}$ | DE = $V_{CC}$ | | | 300 | 500 | |
| | | | DE = 0V | | | 230 | 400 | |
| | | MAX483/MAX487, $\overline{RE}$ = 0V or $V_{CC}$ | DE = 5V | MAX483 | | 350 | 650 | |
| | | | | MAX487 | | 250 | 400 | |
| | | | DE = 0V | | | 120 | 250 | |
| Supply Current in Shutdown | $I_{SHDN}$ | MAX481/483/487, DE = 0V, $\overline{RE}$ = $V_{CC}$ | | | | 0.1 | 10 | µA |
| Driver Short-Circuit Current, $V_O$ = High | $I_{OSD1}$ | -7V ≤ $V_O$ ≤12V (Note 4) | | | 35 | | 250 | mA |
| Driver Short-Circuit Current, $V_O$ = Low | $I_{OSD2}$ | -7V ≤ $V_O$ ≤12V (Note 4) | | | 35 | | 250 | mA |
| Receiver Short-Circuit Current | $I_{OSR}$ | 0V ≤ $V_O$ ≤ $V_{CC}$ | | | 7 | | 95 | mA |

## SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487

($V_{CC}$ = 5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Driver Input to Output | $t_{PLH}$ | Figures 6 and 8, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | | 10 | 30 | 60 | ns |
| | $t_{PHL}$ | | | 10 | 30 | 60 | |
| Driver Output Skew to Output | $t_{SKEW}$ | Figures 6 and 8, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | | | 5 | 10 | ns |
| Driver Rise or Fall Time | $t_R$, $t_F$ | Figures 6 and 8, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | MAX481, MAX485, MAX1487 | 3 | 15 | 40 | ns |
| | | | MAX490C/E, MAX491C/E | 5 | 15 | 25 | |
| | | | MAX490M, MAX491M | 3 | 15 | 40 | |
| Driver Enable to Output High | $t_{ZH}$ | Figures 7 and 9, $C_L$ = 100pF, S2 closed | | | 40 | 70 | ns |
| Driver Enable to Output Low | $t_{ZL}$ | Figures 7 and 9, $C_L$ = 100pF, S1 closed | | | 40 | 70 | ns |
| Driver Disable Time from Low | $t_{LZ}$ | Figures 7 and 9, $C_L$ = 15pF, S1 closed | | | 40 | 70 | ns |
| Driver Disable Time from High | $t_{HZ}$ | Figures 7 and 9, $C_L$ = 15pF, S2 closed | | | 40 | 70 | ns |
| Receiver Input to Output | $t_{PLH}$, $t_{PHL}$ | Figures 6 and 10, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | MAX481, MAX485, MAX1487 | 20 | 90 | 200 | ns |
| | | | MAX490C/E, MAX491C/E | 20 | 90 | 150 | |
| | | | MAX490M, MAX491M | 20 | 90 | 200 | |
| $\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew | $t_{SKD}$ | Figures 6 and 10, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | | | 13 | | ns |
| Receiver Enable to Output Low | $t_{ZL}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S1 closed | | | 20 | 50 | ns |
| Receiver Enable to Output High | $t_{ZH}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S2 closed | | | 20 | 50 | ns |
| Receiver Disable Time from Low | $t_{LZ}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S1 closed | | | 20 | 50 | ns |
| Receiver Disable Time from High | $t_{HZ}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S2 closed | | | 20 | 50 | ns |
| Maximum Data Rate | $f_{MAX}$ | | | 2.5 | | | Mbps |
| Time to Shutdown | $t_{SHDN}$ | MAX481 (Note 5) | | 50 | 200 | 600 | ns |

# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

## SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491, MAX1487 (continued)

($V_{CC}$ = 5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Driver Enable from Shutdown to Output High (MAX481) | $t_{ZH(SHDN)}$ | Figures 7 and 9, $C_L$ = 100pF, S2 closed | | 40 | 100 | ns |
| Driver Enable from Shutdown to Output Low (MAX481) | $t_{ZL(SHDN)}$ | Figures 7 and 9, $C_L$ = 100pF, S1 closed | | 40 | 100 | ns |
| Receiver Enable from Shutdown to Output High (MAX481) | $t_{ZH(SHDN)}$ | Figures 5 and 11, $C_L$ = 15pF, S2 closed, A - B = 2V | | 300 | 1000 | ns |
| Receiver Enable from Shutdown to Output Low (MAX481) | $t_{ZL(SHDN)}$ | Figures 5 and 11, $C_L$ = 15pF, S1 closed, B - A = 2V | | 300 | 1000 | ns |

## SWITCHING CHARACTERISTICS—MAX483, MAX487/MAX488/MAX489

($V_{CC}$ = 5V ±5%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Driver Input to Output | $t_{PLH}$ | Figures 6 and 8, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | 250 | 800 | 2000 | ns |
| | $t_{PHL}$ | | 250 | 800 | 2000 | |
| Driver Output Skew to Output | $t_{SKEW}$ | Figures 6 and 8, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | | 100 | 800 | ns |
| Driver Rise or Fall Time | $t_R$, $t_F$ | Figures 6 and 8, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | 250 | | 2000 | ns |
| Driver Enable to Output High | $t_{ZH}$ | Figures 7 and 9, $C_L$ = 100pF, S2 closed | 250 | | 2000 | ns |
| Driver Enable to Output Low | $t_{ZL}$ | Figures 7 and 9, $C_L$ = 100pF, S1 closed | 250 | | 2000 | ns |
| Driver Disable Time from Low | $t_{LZ}$ | Figures 7 and 9, $C_L$ = 15pF, S1 closed | 300 | | 3000 | ns |
| Driver Disable Time from High | $t_{HZ}$ | Figures 7 and 9, $C_L$ = 15pF, S2 closed | 300 | | 3000 | ns |
| Receiver Input to Output | $t_{PLH}$ | Figures 6 and 10, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | 250 | | 2000 | ns |
| | $t_{PHL}$ | | 250 | | 2000 | |
| \| $t_{PLH}$ - $t_{PHL}$ \| Differential Receiver Skew | $t_{SKD}$ | Figures 6 and 10, $R_{DIFF}$ = 54Ω, $C_{L1}$ = $C_{L2}$ = 100pF | | 100 | | ns |
| Receiver Enable to Output Low | $t_{ZL}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S1 closed | | 20 | 50 | ns |
| Receiver Enable to Output High | $t_{ZH}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S2 closed | | 20 | 50 | ns |
| Receiver Disable Time from Low | $t_{LZ}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S1 closed | | 20 | 50 | ns |
| Receiver Disable Time from High | $t_{HZ}$ | Figures 5 and 11, $C_{RL}$ = 15pF, S2 closed | | 20 | 50 | ns |
| Maximum Data Rate | $f_{MAX}$ | $t_{PLH}$, $t_{PHL}$ < 50% of data period | 250 | | | kbps |
| Time to Shutdown | $t_{SHDN}$ | MAX483/MAX487 (Note 5) | 50 | 200 | 600 | ns |
| Driver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | MAX483/MAX487, Figures 7 and 9, $C_L$ = 100pF, S2 closed | | | 2000 | ns |
| Driver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | MAX483/MAX487, Figures 7 and 9, $C_L$ = 100pF, S1 closed | | | 2000 | ns |
| Receiver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | MAX483/MAX487, Figures 5 and 11, $C_L$ = 15pF, S2 closed | | | 2500 | ns |
| Receiver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | MAX483/MAX487, Figures 5 and 11, $C_L$ = 15pF, S1 closed | | | 2500 | ns |

## NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

**Note 1:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

**Note 2:** All typical specifications are given for $V_{CC}$ = 5V and $T_A$ = +25°C.

**Note 3:** Supply current specification is valid for loaded transmitters when DE = 0V.

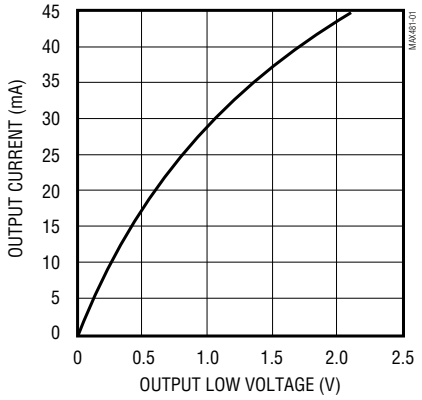
**Note 4:** Applies to peak current. See *Typical Operating Characteristics.*

**Note 5:** The MAX481/MAX483/MAX487 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

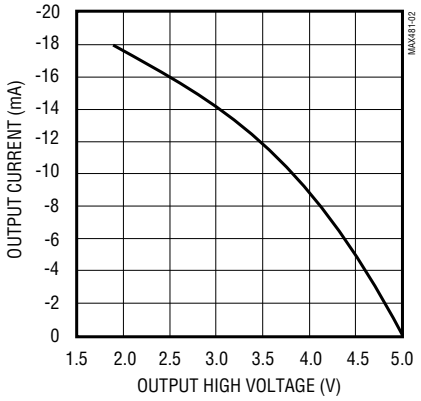
## Typical Operating Characteristics

($V_{CC}$ = 5V, $T_A$ = +25°C, unless otherwise noted.)

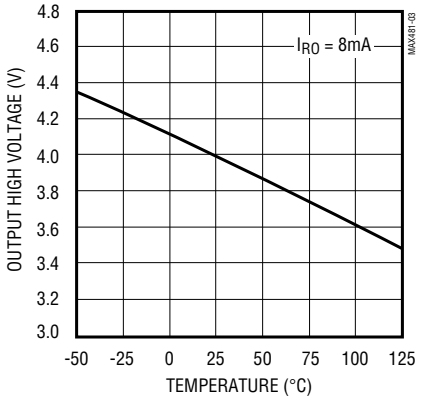
**OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE**



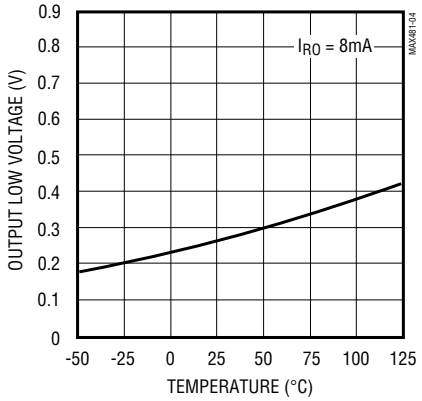

**OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE**



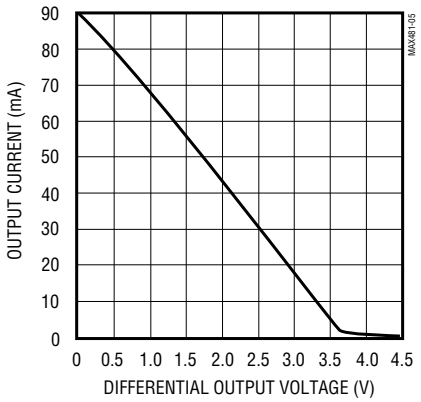

**RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE**



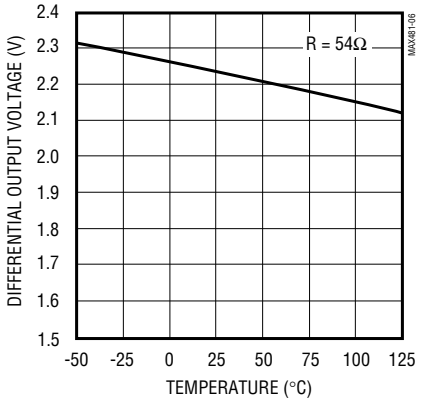

**RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE**




**DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE**




**DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE**

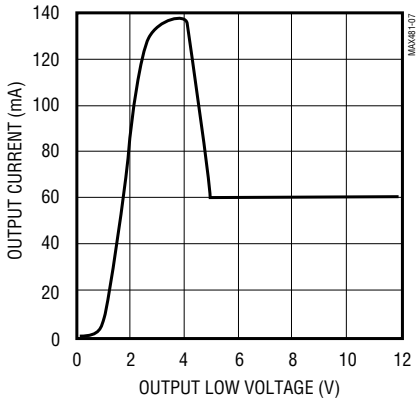


# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

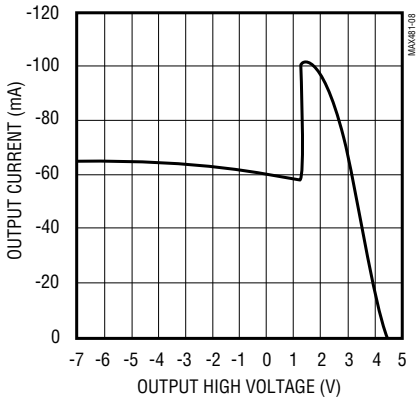
## Typical Operating Characteristics (continued)

($V_{CC}$ = 5V, $T_A$ = +25°C, unless otherwise noted.)

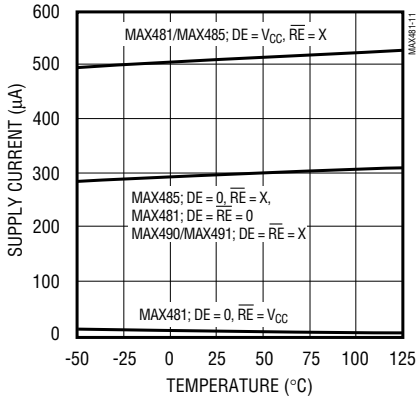
**OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE**



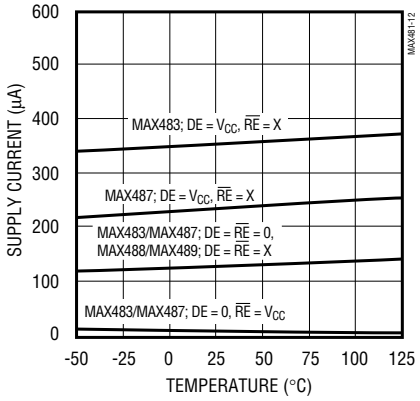

**OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE**



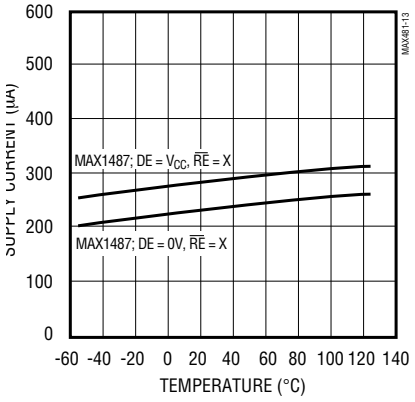

**MAX481/MAX485/MAX490/MAX491 SUPPLY CURRENT vs. TEMPERATURE**




**MAX483/MAX487–MAX489 SUPPLY CURRENT vs. TEMPERATURE**




**MAX1487 SUPPLY CURRENT vs. TEMPERATURE**



## Pin Description

| PIN | | | | | NAME | FUNCTION |
|---|---|---|---|---|---|---|
| MAX481/MAX483/ MAX485/MAX487/ MAX1487 | | MAX488/ MAX490 | | MAX489/ MAX491 | | |
| DIP/SO | µMAX | DIP/SO | µMAX | DIP/SO | | |
| 1 | 3 | 2 | 4 | 2 | RO | Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low. |
| 2 | 4 | — | — | 3 | $\overline{RE}$ | Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. |
| 3 | 5 | — | — | 4 | DE | Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low. |
| 4 | 6 | 3 | 5 | 5 | DI | Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low. |
| 5 | 7 | 4 | 6 | 6, 7 | GND | Ground |
| — | — | 5 | 7 | 9 | Y | Noninverting Driver Output |
| — | — | 6 | 8 | 10 | Z | Inverting Driver Output |
| 6 | 8 | — | — | — | A | Noninverting Receiver Input and Noninverting Driver Output |
| — | — | 8 | 2 | 12 | A | Noninverting Receiver Input |
| 7 | 1 | — | — | — | B | Inverting Receiver Input and Inverting Driver Output |
| — | — | 7 | 1 | 11 | B | Inverting Receiver Input |
| 8 | 2 | 1 | 3 | 14 | $V_{CC}$ | Positive Supply: 4.75V ≤ $V_{CC}$ ≤ 5.25V |
| — | — | — | — | 1, 8, 13 | N.C. | No Connect—not internally connected |

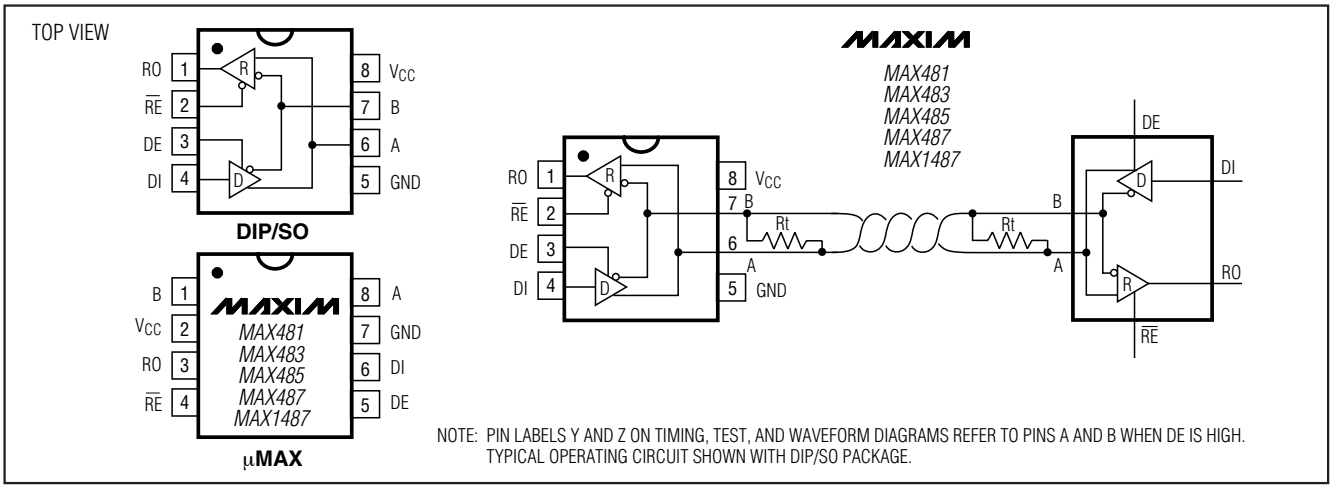



*Figure 1. MAX481/MAX483/MAX485/MAX487/MAX1487 Pin Configuration and Typical Operating Circuit*

# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

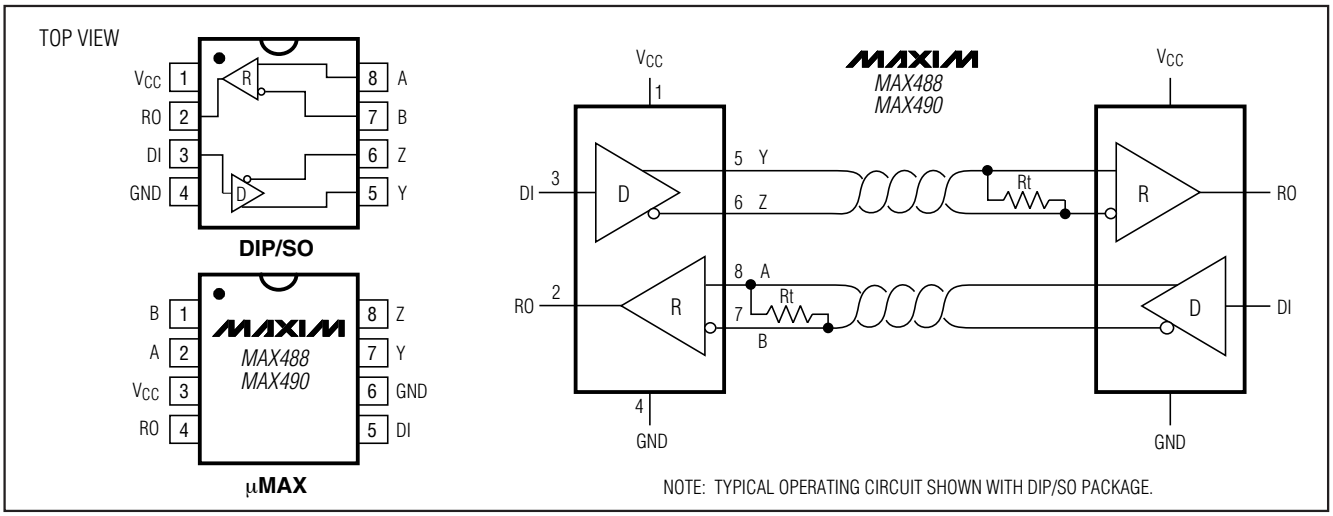



*Figure 2. MAX488/MAX490 Pin Configuration and Typical Operating Circuit*

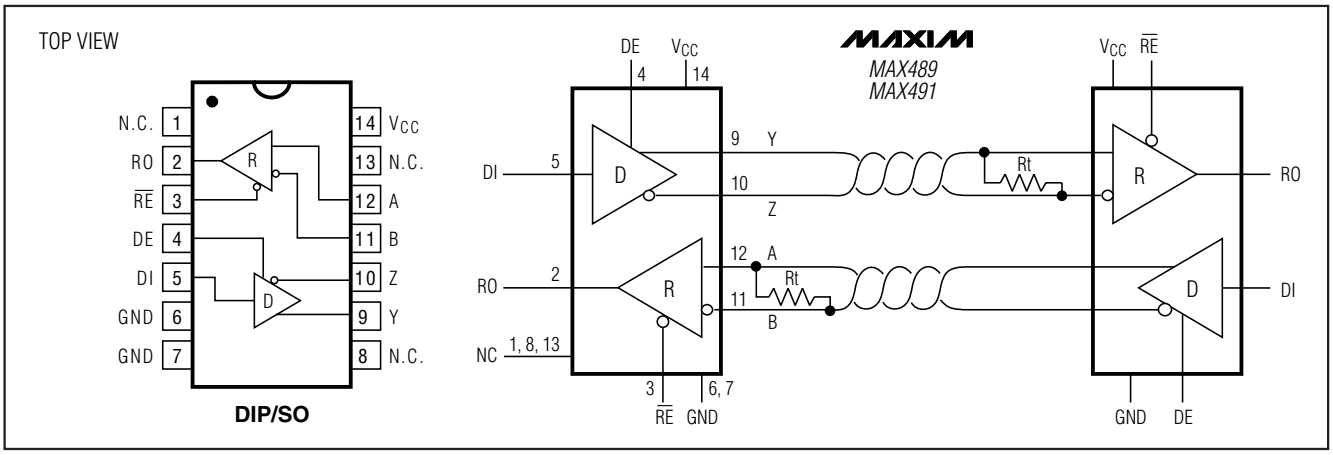



*Figure 3. MAX489/MAX491 Pin Configuration and Typical Operating Circuit*

## Applications Information

The MAX481/MAX483/MAX485/MAX487–MAX491 and MAX1487 are low-power transceivers for RS-485 and RS-422 communications. The MAX481, MAX485, MAX490, MAX491, and MAX1487 can transmit and receive at data rates up to 2.5Mbps, while the MAX483, MAX487, MAX488, and MAX489 are specified for data rates up to 250kbps. The MAX488–MAX491 are full-duplex transceivers while the MAX481, MAX483, MAX485, MAX487, and MAX1487 are half-duplex. In addition, Driver Enable (DE) and Receiver Enable ($\overline{RE}$) pins are included on the MAX481, MAX483, MAX485, MAX487, MAX489, MAX491, and MAX1487. When disabled, the driver and receiver outputs are high impedance.

### MAX487/MAX1487: 128 Transceivers on the Bus

The 48kΩ, $^1/_4$-unit-load receiver input impedance of the MAX487 and MAX1487 allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487/MAX1487 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481/MAX483/MAX485 and MAX488–MAX491 have standard 12kΩ Receiver Input impedance.

## Test Circuits

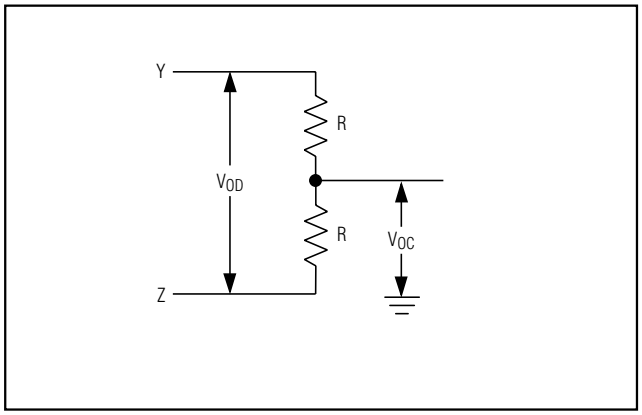



Figure 4. Driver DC Test Load

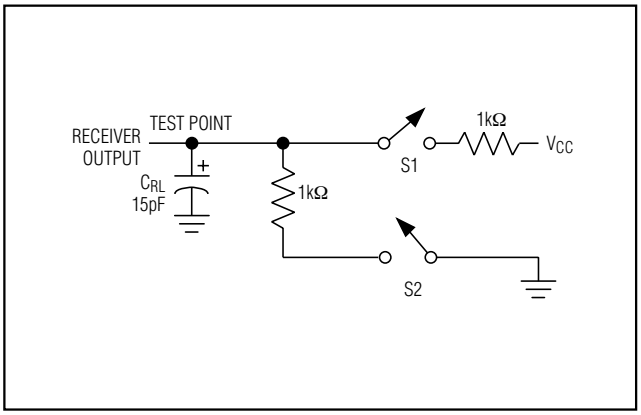



Figure 5. Receiver Timing Test Load

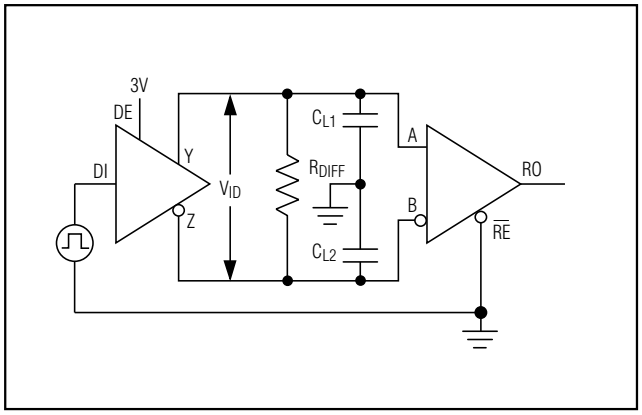



Figure 6. Driver/Receiver Timing Test Circuit

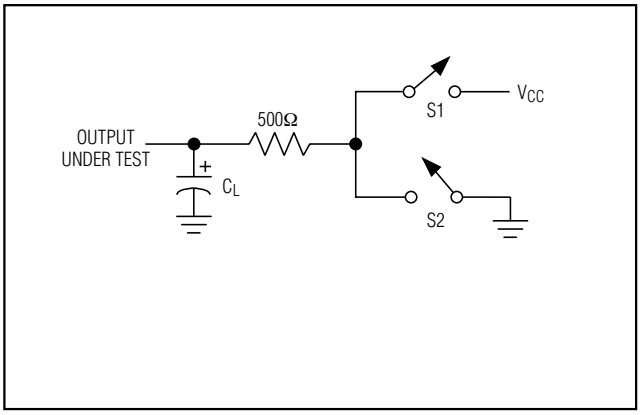



Figure 7. Driver Timing Test Load

### MAX483/MAX487/MAX488/MAX489: Reduced EMI and Reflections

The MAX483 and MAX487–MAX489 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 12 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481, MAX485, MAX490, MAX491, or MAX1487. High-frequency harmonics with large amplitudes are evident. Figure 13 shows the same information displayed for a MAX483, MAX487, MAX488, or MAX489 transmitting under the same conditions. Figure 13's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

## Switching Waveforms

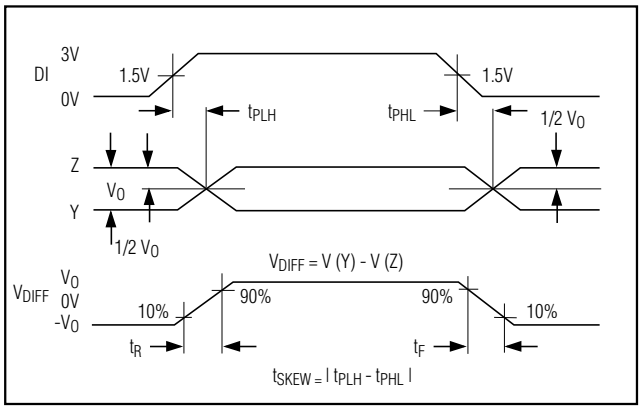



*Figure 8. Driver Propagation Delays*

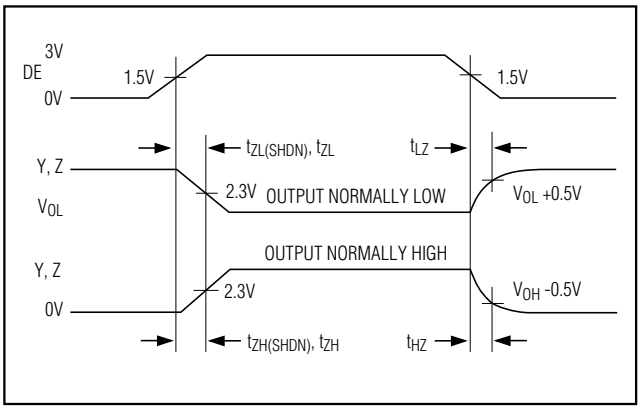



*Figure 9. Driver Enable and Disable Times (except MAX488 and MAX490)*

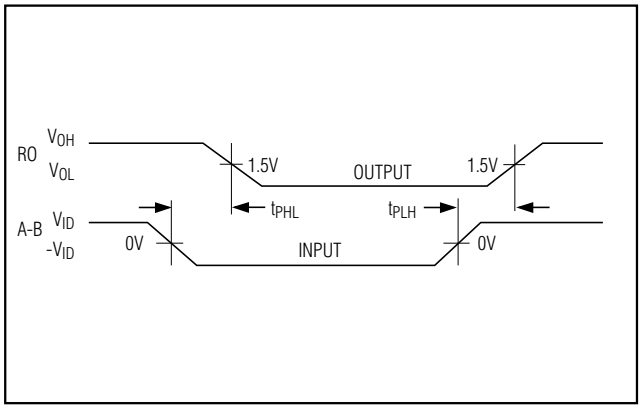



*Figure 10. Receiver Propagation Delays*

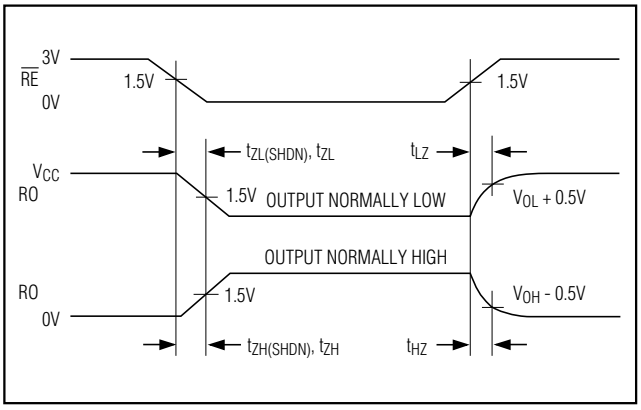



*Figure 11. Receiver Enable and Disable Times (except MAX488 and MAX490)*

## Function Tables (MAX481/MAX483/MAX485/MAX487/MAX1487)

### Table 1. Transmitting

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{RE}$ | DE | DI | Z | Y |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| 0 | 0 | X | High-Z | High-Z |
| 1 | 0 | X | High-Z* | High-Z* |

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

### Table 2. Receiving

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{RE}$ | DE | A-B | RO |
| 0 | 0 | ≥ +0.2V | 1 |
| 0 | 0 | ≤ -0.2V | 0 |
| 0 | 0 | Inputs open | 1 |
| 1 | 0 | X | High-Z* |

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

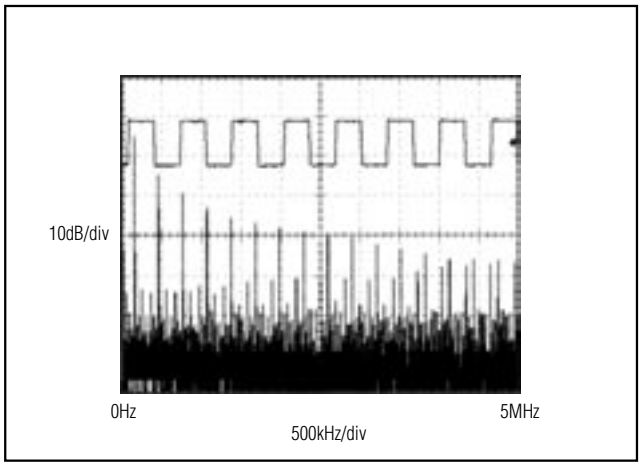



*Figure 12. Driver Output Waveform and FFT Plot of MAX481/ MAX485/MAX490/MAX491/MAX1487 Transmitting a 150kHz Signal*

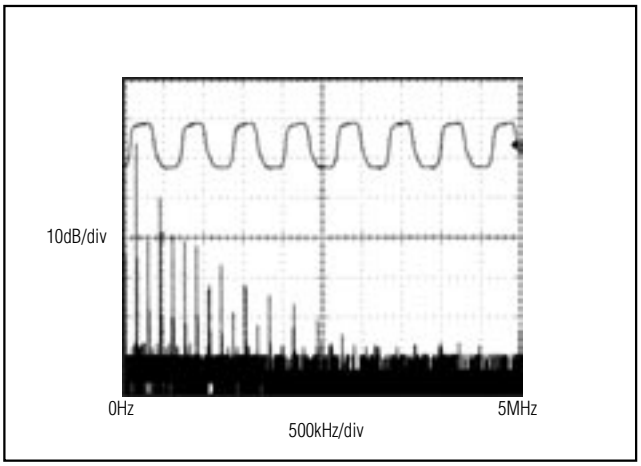



*Figure 13. Driver Output Waveform and FFT Plot of MAX483/ MAX487–MAX489 Transmitting a 150kHz Signal*

### Low-Power Shutdown Mode (MAX481/MAX483/MAX487)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.1µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481, MAX483, and MAX487, the $t_{ZH}$ and $t_{ZL}$ enable times assume the part was not in the low-power shutdown state (the MAX485/MAX488–MAX491 and MAX1487 can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode ($t_{ZH}$, $t_{ZL}$). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

### Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

### Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 15–18 using Figure 14's test circuit.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 13ns for the MAX481, MAX485, MAX490, MAX491, and MAX1487 and is typically less than 100ns for the MAX483 and MAX487–MAX489.

The driver skew times are typically 5ns (10ns max) for the MAX481, MAX485, MAX490, MAX491, and MAX1487, and are typically 100ns (800ns max) for the MAX483 and MAX487–MAX489.

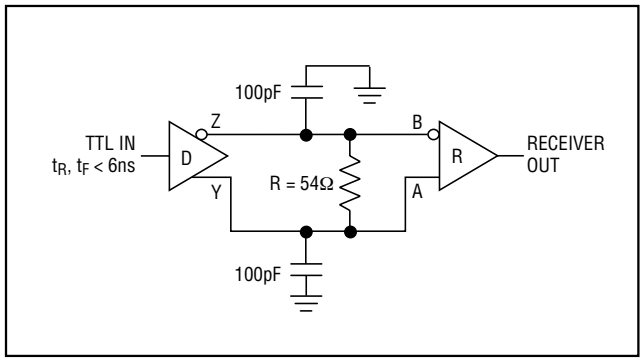



*Figure 14. Receiver Propagation Delay Test Circuit*

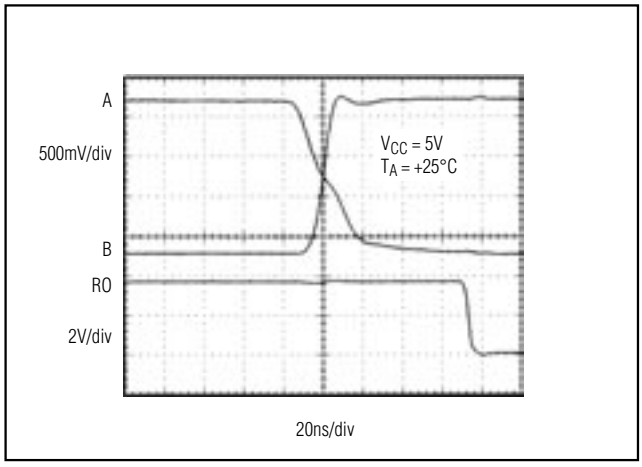



*Figure 15. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver $t_{PHL}$*

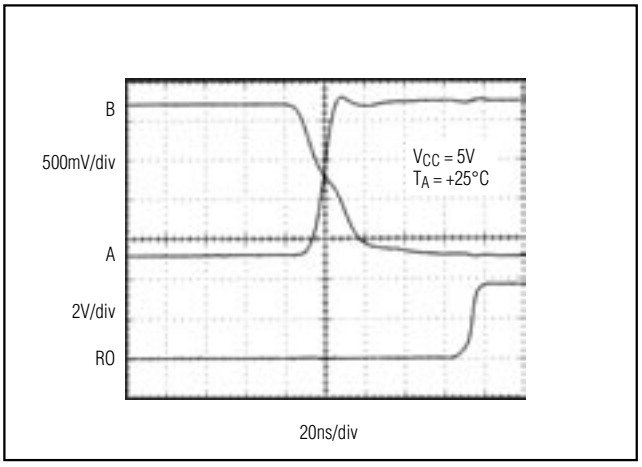



*Figure 16. MAX481/MAX485/MAX490/MAX491/MAX1487 Receiver $t_{PLH}$*

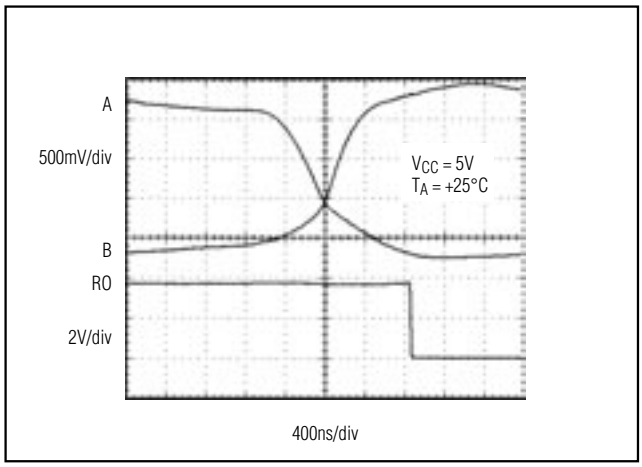



*Figure 17. MAX483, MAX487–MAX489 Receiver $t_{PHL}$*

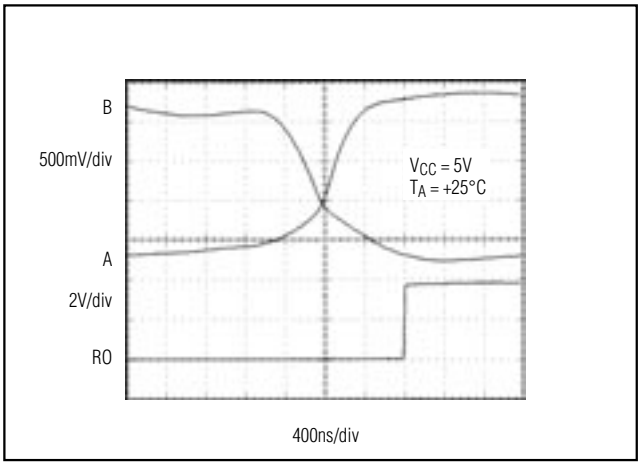



*Figure 18. MAX483, MAX487–MAX489 Receiver $t_{PLH}$*

### Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 23.

Figures 19 and 20 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 120Ω loads.

### Typical Applications

The MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 23.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483 and MAX487–MAX489 are more tolerant of imperfect termination.

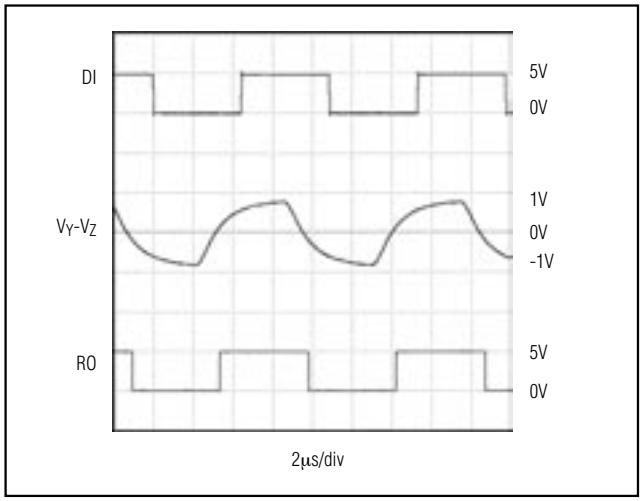



*Figure 19. MAX481/MAX485/MAX490/MAX491/MAX1487 System Differential Voltage at 110kHz Driving 4000ft of Cable*

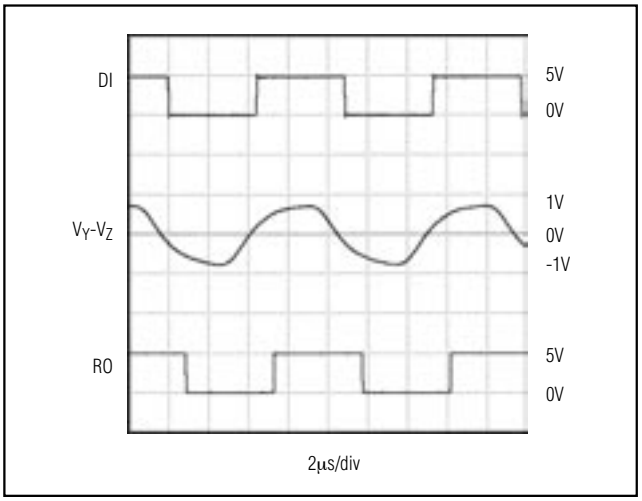



*Figure 20. MAX483, MAX487–MAX489 System Differential Voltage at 110kHz Driving 4000ft of Cable*

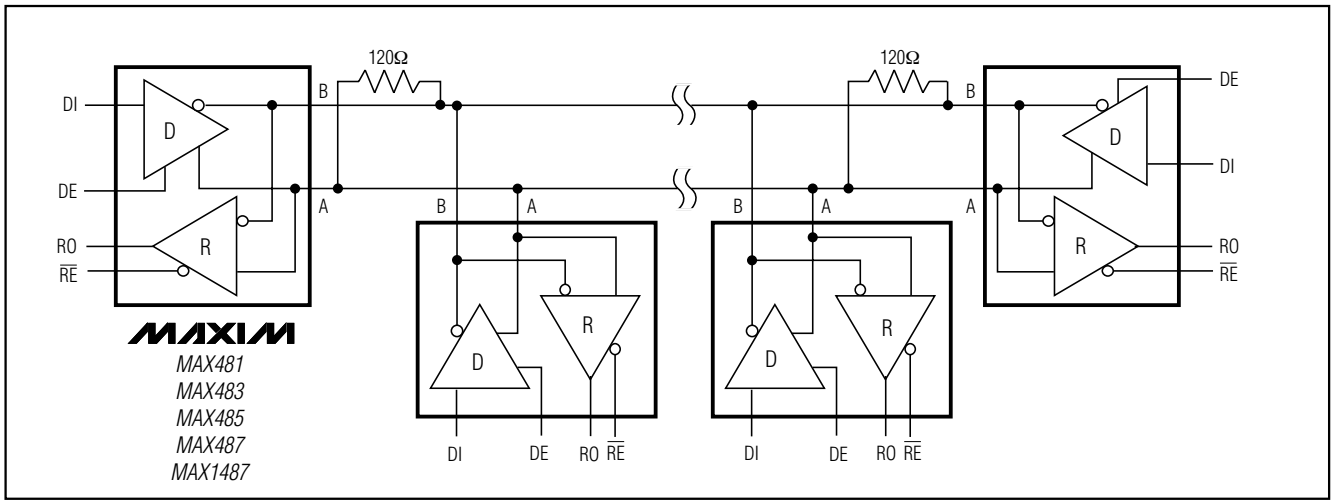



*Figure 21. MAX481/MAX483/MAX485/MAX487/MAX1487 Typical Half-Duplex RS-485 Network*

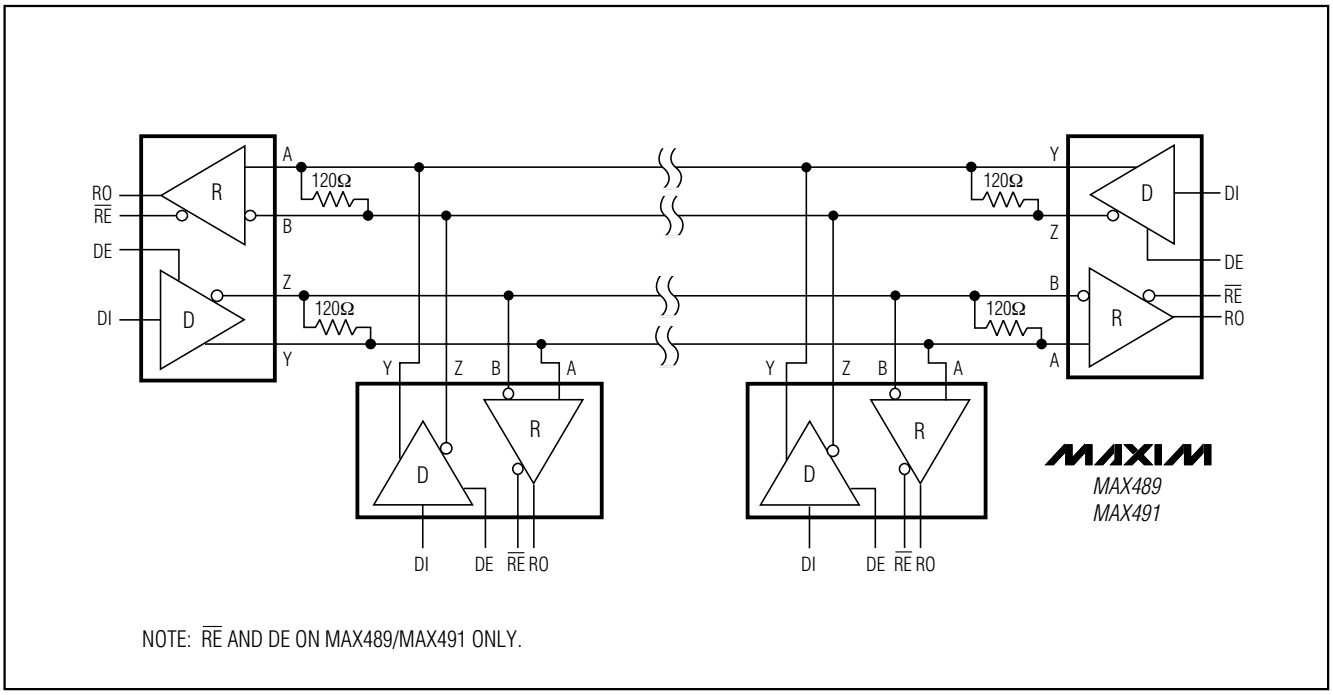



*Figure 22. MAX488–MAX491 Full-Duplex RS-485 Network*

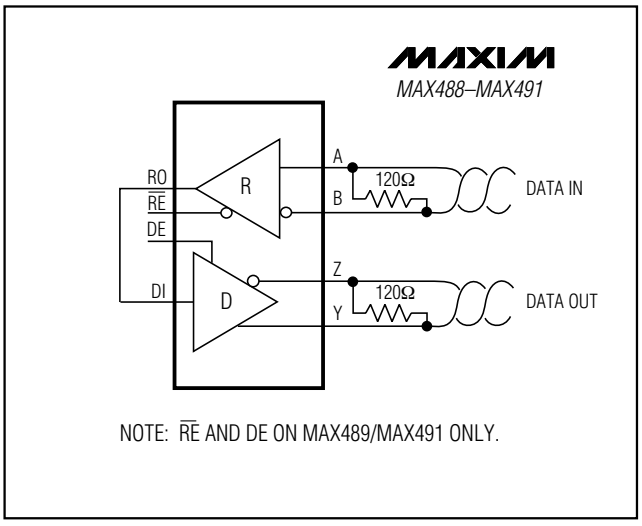



*Figure 23. Line Repeater for MAX488–MAX491*

### Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX481**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX481CSA | 0°C to +70°C | 8 SO |
| MAX481CUA | 0°C to +70°C | 8 µMAX |
| MAX481C/D | 0°C to +70°C | Dice* |
| MAX481EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX481ESA | -40°C to +85°C | 8 SO |
| MAX481MJA | -55°C to +125°C | 8 CERDIP |
| **MAX483**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX483CSA | 0°C to +70°C | 8 SO |
| MAX483CUA | 0°C to +70°C | 8 µMAX |
| MAX483C/D | 0°C to +70°C | Dice* |
| MAX483EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX483ESA | -40°C to +85°C | 8 SO |
| MAX483MJA | -55°C to +125°C | 8 CERDIP |
| **MAX485**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX485CSA | 0°C to +70°C | 8 SO |
| MAX485CUA | 0°C to +70°C | 8 µMAX |
| MAX485C/D | 0°C to +70°C | Dice* |
| MAX485EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX485ESA | -40°C to +85°C | 8 SO |
| MAX485MJA | -55°C to +125°C | 8 CERDIP |
| **MAX487**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX487CSA | 0°C to +70°C | 8 SO |
| MAX487CUA | 0°C to +70°C | 8 µMAX |
| MAX487C/D | 0°C to +70°C | Dice* |
| MAX487EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX487ESA | -40°C to +85°C | 8 SO |
| MAX487MJA | -55°C to +125°C | 8 CERDIP |
| **MAX488**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX488CSA | 0°C to +70°C | 8 SO |
| MAX488CUA | 0°C to +70°C | 8 µMAX |
| MAX488C/D | 0°C to +70°C | Dice* |
| MAX488EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX488ESA | -40°C to +85°C | 8 SO |
| MAX488MJA | -55°C to +125°C | 8 CERDIP |
| **MAX489**CPD | 0°C to +70°C | 14 Plastic DIP |
| MAX489CSD | 0°C to +70°C | 14 SO |
| MAX489C/D | 0°C to +70°C | Dice* |
| MAX489EPD | -40°C to +85°C | 14 Plastic DIP |
| MAX489ESD | -40°C to +85°C | 14 SO |
| MAX489MJD | -55°C to +125°C | 14 CERDIP |

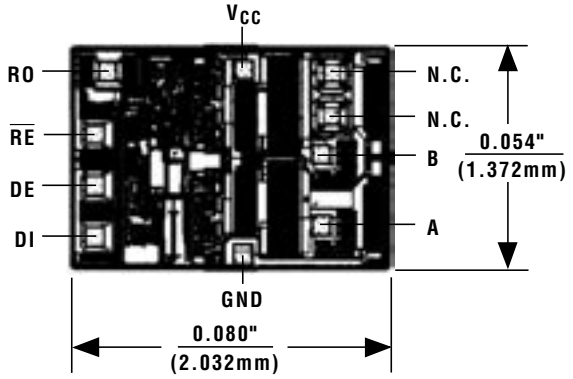
## Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX490**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX490CSA | 0°C to +70°C | 8 SO |
| MAX490CUA | 0°C to +70°C | 8 µMAX |
| MAX490C/D | 0°C to +70°C | Dice* |
| MAX490EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX490ESA | -40°C to +85°C | 8 SO |
| MAX490MJA | -55°C to +125°C | 8 CERDIP |
| **MAX491**CPD | 0°C to +70°C | 14 Plastic DIP |
| MAX491CSD | 0°C to +70°C | 14 SO |
| MAX491C/D | 0°C to +70°C | Dice* |
| MAX491EPD | -40°C to +85°C | 14 Plastic DIP |
| MAX491ESD | -40°C to +85°C | 14 SO |
| MAX491MJD | -55°C to +125°C | 14 CERDIP |
| **MAX1487**CPA | 0°C to +70°C | 8 Plastic DIP |
| MAX1487CSA | 0°C to +70°C | 8 SO |
| MAX1487CUA | 0°C to +70°C | 8 µMAX |
| MAX1487C/D | 0°C to +70°C | Dice* |
| MAX1487EPA | -40°C to +85°C | 8 Plastic DIP |
| MAX1487ESA | -40°C to +85°C | 8 SO |
| MAX1487MJA | -55°C to +125°C | 8 CERDIP |

** Contact factory for dice specifications.*

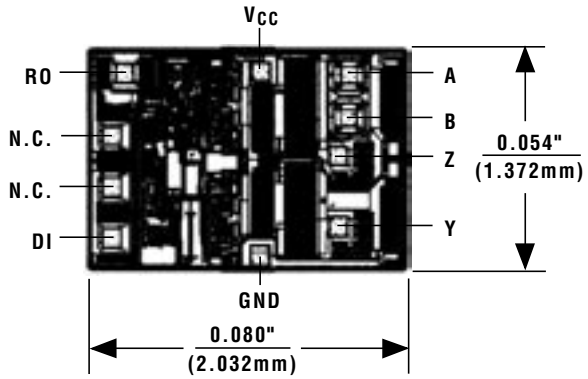
## Chip Topographies

**MAX481/MAX483/MAX485/MAX487/MAX1487**

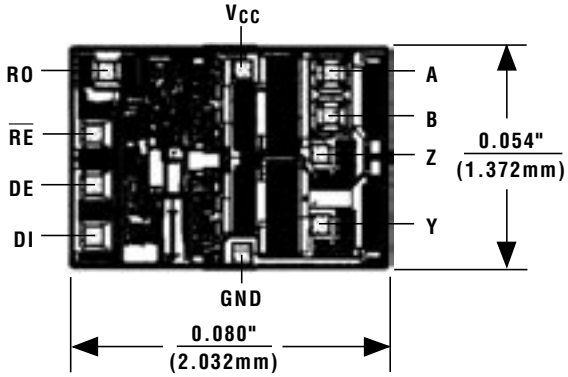


## Chip Topographies (continued)

**MAX488/MAX490**




**MAX489/MAX491**




TRANSISTOR COUNT: 248

SUBSTRATE CONNECTED TO GND

## Package Information

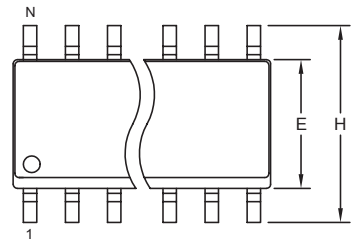
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

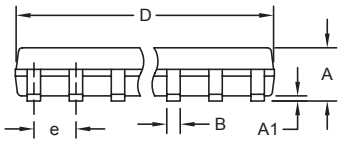
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

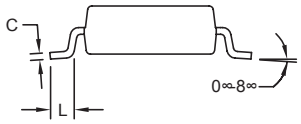
| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | N | MS012 |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |




TOP VIEW




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

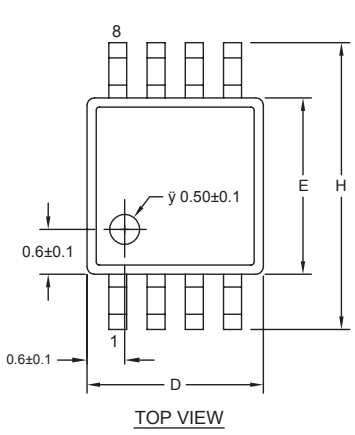
| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

# Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

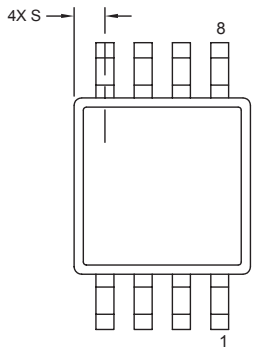
## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

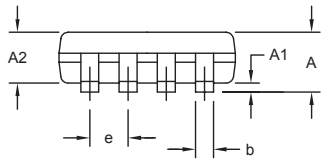



TOP VIEW

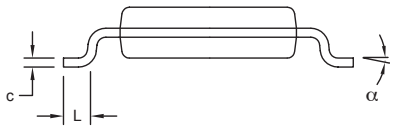



BOTTOM VIEW

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | - | 0.043 | - | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 |
| b | 0.010 | 0.014 | 0.25 | 0.36 |
| c | 0.005 | 0.007 | 0.13 | 0.18 |
| D | 0.116 | 0.120 | 2.95 | 3.05 |
| e | 0.0256 BSC | | 0.65 BSC | |
| E | 0.116 | 0.120 | 2.95 | 3.05 |
| H | 0.188 | 0.198 | 4.78 | 5.03 |
| L | 0.016 | 0.026 | 0.41 | 0.66 |
| α | 0∞ | 6∞ | 0∞ | 6∞ |
| S | 0.0207 BSC | | 0.5250 BSC | |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

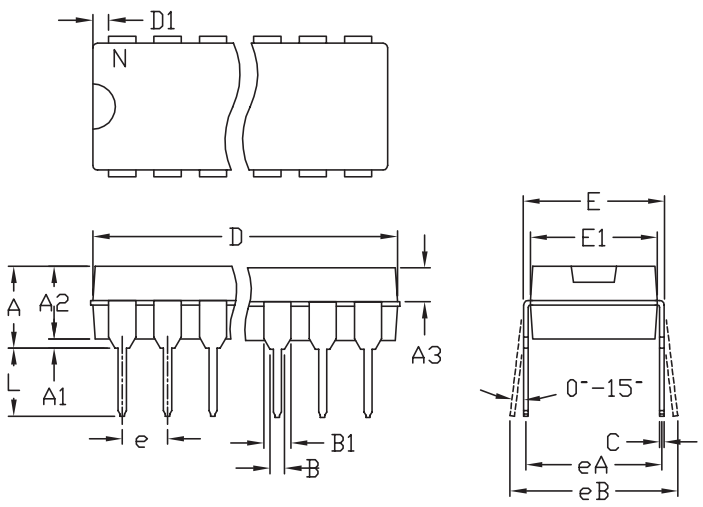
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0036 | J | 1/1 |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.180 | --- | 4.572 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.015 | 0.022 | 0.381 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.014 | 0.2 | 0.355 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 BSC. | | 2.54 BSC. | |
| eA | 0.300 BSC. | | 7.62 BSC. | |
| eB | 0.400 BSC. | | 10.16 BSC. | |
| L | 0.115 | 0.150 | 2.921 | 3.81 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS001 |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: PDIP .300"
TITLE

1/1

21-0043 D
DOCUMENT CONTROL NUMBER REV

# MC78TXX

## 3-Terminal 3A Positive Voltage Regulator

### Features

- Output current in excess of 3.0A
- Output transistor safe operating area compensation
- Power dissipation :25W
- Internal short circuit current limiting
- Internal thermal overload protection
- Output voltage offered in 4% tolerance
- No external components required
- Output voltage of 5,12 and 15V

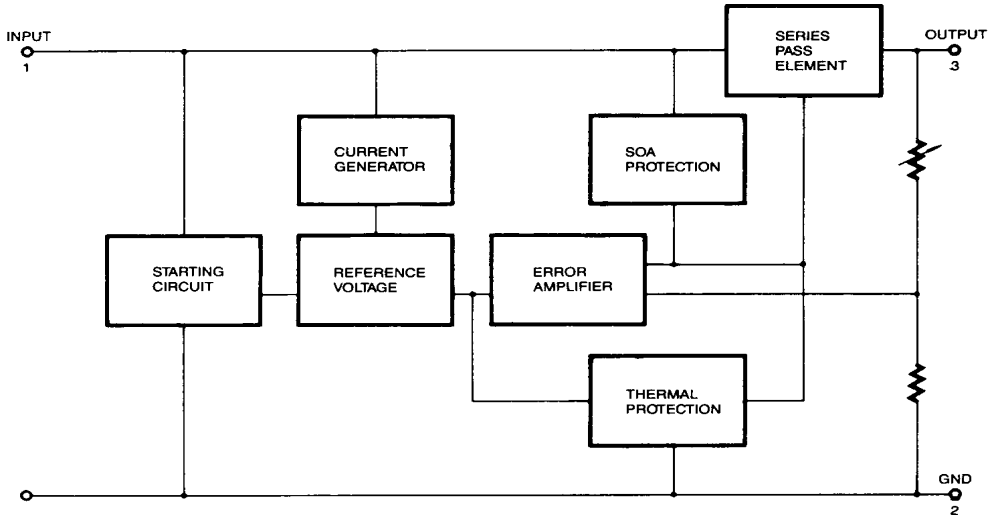
### Description

This family of fixed voltage regulators are monolithic integrated circuit capable of driving loads in excess of 3.0 A.

**TO-220**


1.Input 2. GND 3. Output

### Internal Block Diagram




Rev. 1.0.0

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (for $V_O$ = 5V to 12V)<br>(for $V_O$ = 15V) | $V_I$ | 35<br>40 | V<br>V |
| Power Dissipation | PD | Internally limited | |
| Thermal Resistance, Junction to Air<br>Tc = +25 °C | RθJA | 65 | °C/W |
| Thermal Resistance ,Junction to Case | RθJC | 2.5 | °C/W |
| Operating Junction Temperature Range | $T_J$ | 0 ~ +150 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 ~ +150 | °C |

## Electrical Characteristics(MC78T05)

($V_I$ = 10V, $I_O$ = 3.0 A, 0 °C ≤ $T_J$ ≤ +125 °C, Po ≤ $P_{MAX}$ , unless otherwise specified. )

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | Vo | 5mA ≤ Io ≤ 3.0A , $T_J$ = +25 °C<br>7.3V ≤ VI ≤ 20V, 5mA ≤ Io ≤ 2.0A | 4.8<br>4.75 | 5.0<br>5.0 | 5.2<br>5.25 | V |
| Line Regulation (Note1) | $\Delta V_O$ | 7.2V ≤ VI ≤ 35V , Io=5mA, $T_J$ =+25 °C<br>7.2V ≤ VI ≤ 35V , Io=1.0A, $T_J$ = +25 °C<br>7.5V ≤ VI ≤ 20V, Io =2.0A<br>8.0V ≤ VI ≤ 12V, Io =3.0A | - | 3.0 | 2.5 | mV |
| Load Regulation (Note1) | $\Delta V_O$ | 5mA ≤ Io ≤ 3.0A , $T_J$ = +25 °C<br>5mA ≤ Io ≤ 3.0A | - | 10<br>15 | 30<br>80 | mV<br>mV |
| Thermal Regulation | $REG_T$ | Pulse =10ms, P = 20W<br>TA = +25 °C | - | 0.002 | 0.03 | %Vo/W |
| Quiescent Current | $I_Q$ | 5mA ≤ Io ≤ 3.0A , $T_J$ = +25 °C<br>5mA ≤ Io ≤ 3.0A | - | 3.5<br>4.0 | 5.0<br>6.0 | mA<br>mA |
| Quiescent Current Change | $\Delta I_Q$ | 7.2V ≤ VI ≤ 35V, Io = 5mA<br>$T_J$ = +25 °C ;<br>7.5V ≤ VI ≤ 20V, Io =2.0A ;<br>5mA ≤ Io ≤ 3.0A | - | 0.1 | 0.8 | mA |
| Ripple Rejection | RR | f = 120Hz, 8V ≤ $V_I$ ≤ 18V, $I_O$ = 2.0A | - | 75 | - | dB |
| Dropout Voltage | $V_D$ | Io = 3A ,$T_J$ = +25 °C | - | 2.2 | 2.5 | V |
| Output Noise Voltage | $V_N$ | $T_A$ = +25 °C, 10Hz ≤ f ≤ 100KHz | - | 10 | - | μV/Vo |
| Peak Output Current | $I_{PK}$ | $T_A$ = +25 °C | - | 5.0 | - | A |
| Output Resistance | Ro | f = 1.0kHz | - | 2.0 | - | m Ω |
| Short Circuit Current Limit | Isc | VI = 35V, $T_J$ =+25 °C | - | 1.5 | 2.5 | A |
| Average Temperature Coefficient of Output Voltage | $\Delta V_O/\Delta T$ | Io = 5.0mA | - | 0.2 | - | mV/°C |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in Vo due heating effects must be taken into account separately. Pulse testing with low duty is used .( $P_{MAX}$ = 25W)

## Electrical Characteristics(MC78T12)

($V_I$ = 19V, $I_O$ = 3.0 A, 0 °C ≤ $T_J$ ≤ +125 °C, Po ≤ $P_{MAX}$ , unless otherwise specified. )

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | Vo | 5mA ≤ Io ≤ 3.0A , $T_J$ =+25 °C<br>14.5V ≤ VI ≤ 27V, 5mA ≤ Io ≤ 2.0A | 11.5<br>11.4 | 12<br>12 | 12.5<br>12.8 | V |
| Line Regulation (Note1) | $\Delta V_O$ | 14.5V ≤ VI ≤ 35V , Io=5mA, $T_J$ =+25 °C<br>14.5V ≤ VI ≤ 35V , Io=1.0A, $T_J$ =+25 °C<br>14.9V ≤ VI ≤ 28V, Io =2.0A<br>16V ≤ VI ≤ 22V, Io =3.0A | - | 6.0 | 45 | mV |
| Load Regulation (Note1) | $\Delta V_O$ | 5mA ≤ Io ≤ 3.0A , $T_J$ =+25 °C<br>5mA ≤ Io ≤ 3.0A | - | 10<br>15 | 30<br>80 | mV<br>mV |
| Thermal Regulation | $REG_T$ | Pulse =10ms, P = 20W<br>TA = +25 °C | - | 0.002 | 0.03 | %Vo/W |
| Quiescent Current | $I_Q$ | 5mA ≤ Io ≤ 3.0A , $T_J$ =+25 °C<br>5mA ≤ Io ≤ 3.0A | - | 3.5<br>4.0 | 5.0<br>6.0 | mA<br>mA |
| Quiescent Current Change | $\Delta I_Q$ | 14.5V ≤ VI ≤ 35V, Io = 5mA<br>$T_J$ =+25 °C ;<br>14.9V ≤ VI ≤ 27V, Io =2.0A ;<br>5mA ≤ Io ≤ 3.0A | - | 0.1 | 0.8 | mA |
| Ripple Rejection | RR | f = 120Hz, 15V ≤ $V_I$ ≤ 25V, Io = 2.0A | 57 | 67 | - | dB |
| Dropout Voltage | $V_D$ | Io = 3A ,$T_J$ =+25 °C | - | 2.2 | 2.5 | V |
| Output Noise Voltage | $V_N$ | $T_A$ =+25 °C, 10Hz ≤ f ≤ 100KHz | - | 10 | - | μV/Vo |
| Peak Output Current | $I_{PK}$ | $T_A$ =+25 °C | - | 5.0 | - | A |
| Output Resistance | Ro | f = 1.0kHz | - | 2.0 | - | mΩ |
| Short Circuit Current Limit | Isc | VI = 35V, $T_J$ =+25 °C | - | 1.5 | 2.5 | A |
| Average Temperature Coefficient of Output Voltage | $\Delta V_O/\Delta T$ | Io = 5.0mA | - | 0.5 | - | mV/°C |

- Load and line regulation are specified at constant junction temperature. Change in Vo due heating effects must be taken into account separately. Pulse testing with low duty is used .( $P_{MAX}$ = 25W)

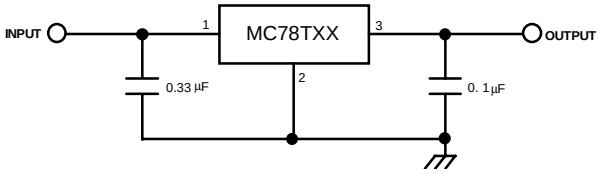
## Electrical Characteristics(MC78T15)

($V_I$ = 23V, $I_O$ = 3.0 A, 0 °C ≤ $T_J$ ≤ +125 °C, Po ≤ $P_{MAX}$ , unless otherwise specified. )

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | Vo | 5mA ≤ Io ≤ 3.0A , $T_J$ =+25 °C<br>17.5V ≤ VI ≤ 30V, 5mA ≤ Io ≤ 2.0A | 14.4<br>14.25 | 15<br>15 | 15.6<br>15.75 | V |
| Line Regulation (Note1) | $\Delta V_O$ | 17.6V ≤ VI ≤ 40V , Io=5mA, $T_J$ =+25 °C<br>17.6V ≤ VI ≤ 40V , Io=1.0A, $T_J$ =+25 °C<br>18V ≤ VI ≤ 30V, Io =2.0A<br>20V ≤ VI ≤ 26V, Io =3.0A | - | 7.5 | 55 | mV |
| Load Regulation (Note1) | $\Delta V_O$ | 5mA ≤ Io ≤ 3.0A , $T_J$ =+25 °C<br>5mA ≤ Io ≤ 3.0A | - | 10<br>15 | 30<br>80 | mV<br>mV |
| Thermal Regulation | $REG_T$ | Pulse =10ms, P = 20W<br>TA = +25 °C | - | 0.002 | 0.03 | %Vo/W |
| Quiescent Current | $I_Q$ | 5mA ≤ Io ≤ 3.0A , $T_J$ =+25 °C<br>5mA ≤ Io ≤ 3.0A | - | 3.5<br>4.0 | 5.0<br>6.0 | mA<br>mA |
| Quiescent Current Change | $\Delta I_Q$ | 17.6V ≤ VI ≤ 40V, Io = 5mA<br>$T_J$ =+25 °C ;<br>18V ≤ VI ≤ 30V, Io =2.0A ;<br>5mA ≤ Io ≤ 3.0A | - | 0.1 | 0.8 | mA |
| Ripple Rejection | RR | f = 120Hz, 18.5V ≤ $V_I$ ≤ 28.5V, Io = 2.0A | 55 | 65 | - | dB |
| Dropout Voltage | $V_D$ | Io = 3A ,$T_J$ =+25 °C | - | 2.2 | 2.5 | V |
| Output Noise Voltage | $V_N$ | $T_A$ =+25 °C, 10Hz ≤ f ≤ 100KHz | - | 10 | - | μV/Vo |
| Peak Output Current | $I_{PK}$ | $T_A$ =+25 °C | - | 5.0 | - | A |
| Output Resistance | Ro | f = 1.0kHz | - | 2.0 | - | mΩ |
| Short Circuit Current Limit | Isc | VI = 40V, $T_J$ =+25 °C | - | 1.0 | 2.0 | A |
| Average Temperature Coefficient of Output Voltage | $\Delta V_O/\Delta T$ | Io = 5.0mA | - | 0.5 | - | mV/°C |

- Load and line regulation are specified at constant junction temperature. Change in Vo due heating effects must be taken into account separately. Pulse testing with low duty is used .( $P_{MAX}$ = 25W)

## Typical Application



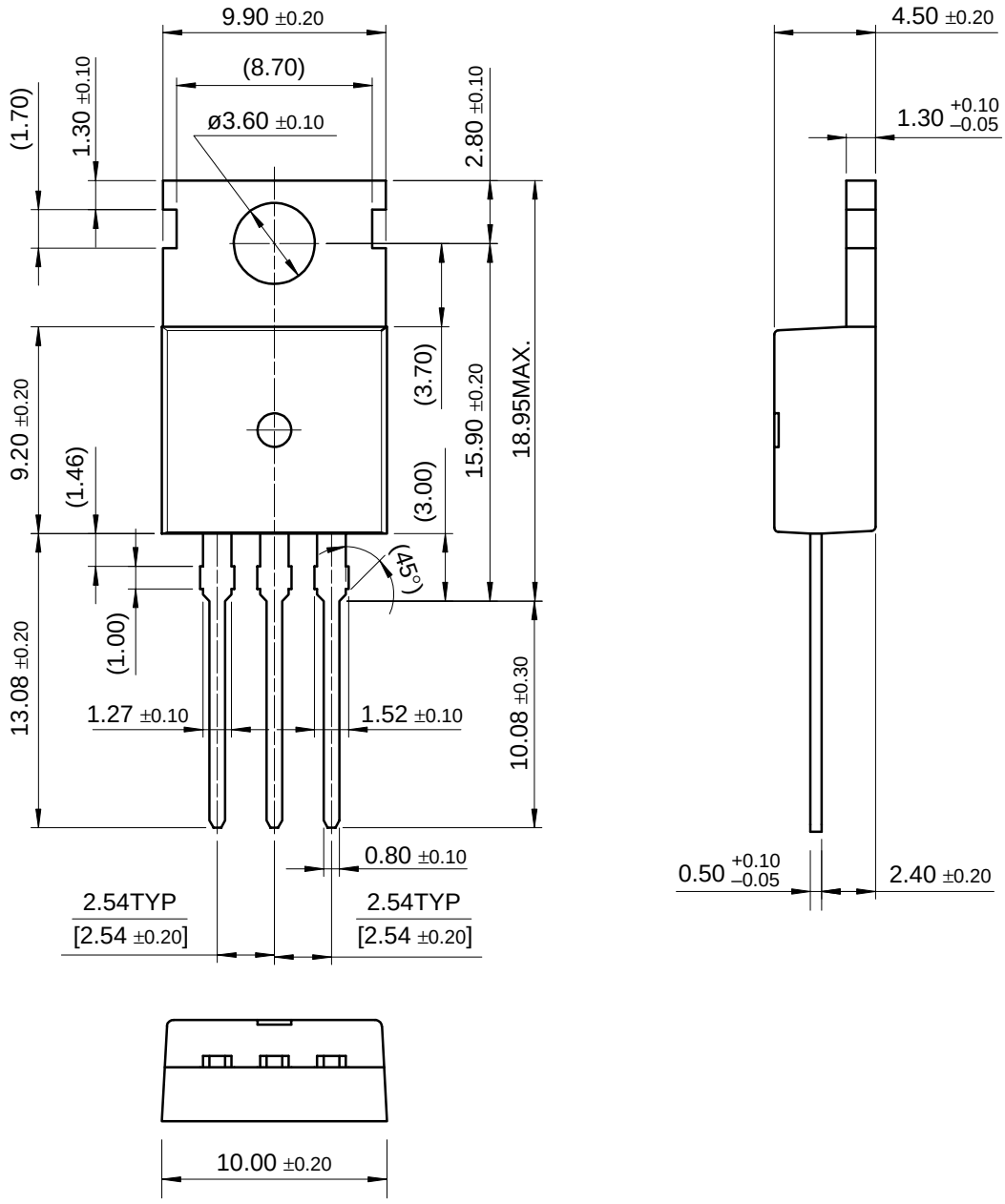

**Notes:**

1. To specify an output voltage, substitute voltage value for “XX”.
2. Bypass Capacitors are recommend for optimum stability and transient response and should be located as close as possible to the regulator

## Mechanical Dimensions

### Package

# TO-220



## Ordering Information

| Product Number | Package | Operating Temperature |
|---|---|---|
| MC78T05CT | TO-220 | 0 ~ + 125 °C |
| MC78T12CT | | |
| MC78T15CT | | |

# MC78XX/LM78XX/MC78XXA

## 3-Terminal 1A Positive Voltage Regulator

### Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

### Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

**TO-220**

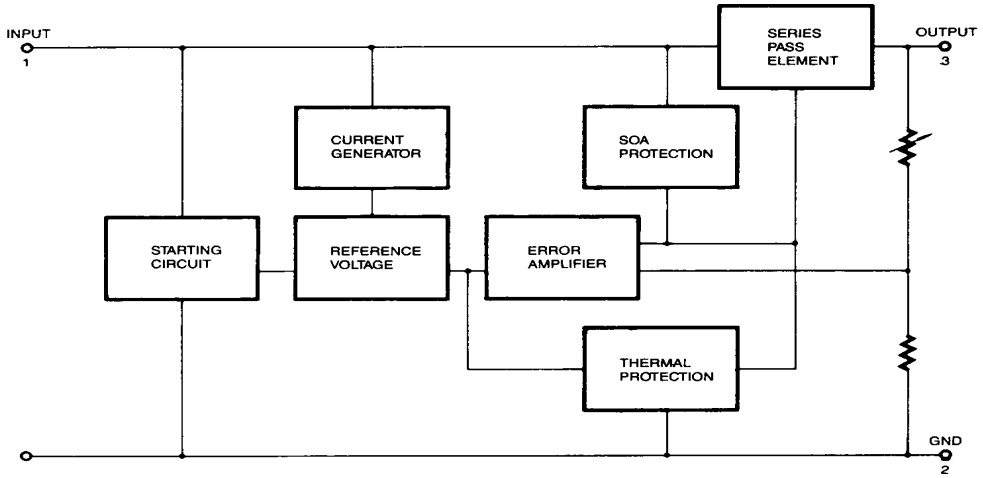
1

**D-PAK**

1

1. Input 2. GND 3. Output

### Internal Block Digram




Rev. 1.0.1

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (for $V_O$ = 5V to 18V)<br>(for $V_O$ = 24V) | $V_I$<br>$V_I$ | 35<br>40 | V<br>V |
| Thermal Resistance Junction-Cases (TO-220) | $R_{\theta JC}$ | 5 | $^oC/W$ |
| Thermal Resistance Junction-Air (TO-220) | $R_{\theta JA}$ | 65 | $^oC/W$ |
| Operating Temperature Range | $T_{OPR}$ | 0 ~ +125 | $^oC$ |
| Storage Temperature Range | $T_{STG}$ | -65 ~ +150 | $^oC$ |

## Electrical Characteristics (MC7805/LM7805)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ = 10V, $C_I$= 0.33µF, $C_O$= 0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7805/LM7805 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 $^oC$ | | 4.8 | 5.0 | 5.2 | V |
| | | 5.0mA ≤ Io ≤ 1.0A, $P_O$ ≤ 15W<br>$V_I$ = 7V to 20V | | 4.75 | 5.0 | 5.25 | |
| Line Regulation (Note1) | Regline | $T_J$=+25 $^oC$ | $V_O$ = 7V to 25V | - | 4.0 | 100 | mV |
| | | | $V_I$ = 8V to 12V | - | 1.6 | 50 | |
| Load Regulation (Note1) | Regload | $T_J$=+25 $^oC$ | $I_O$ = 5.0mA to1.5A | - | 9 | 100 | mV |
| | | | $I_O$ =250mA to 750mA | - | 4 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 $^oC$ | | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | 0.03 | 0.5 | mA |
| | | $V_I$= 7V to 25V | | - | 0.3 | 1.3 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$= 5mA | | - | -0.8 | - | mV/ $^oC$ |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$=+25 $^oC$ | | - | 42 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_O$ = 8V to 18V | | 62 | 73 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 $^oC$ | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 15 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$ =+25 $^oC$ | | - | 230 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 $^oC$ | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_o$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7806)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =11V, $C_I$= 0.33µF, $C_O$= 0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7806 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 5.75 | 6.0 | 6.25 | V |
| | | 5.0mA ≤ $I_O$ ≤ 1.0A, $P_O$ ≤ 15W<br>$V_I$ = 8.0V to 21V | | 5.7 | 6.0 | 6.3 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25 °C | $V_I$ = 8V to 25V | - | 5 | 120 | mV |
| | | | $V_I$ = 9V to 13V | - | 1.5 | 60 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C | $I_O$ =5mA to 1.5A | - | 9 | 120 | mV |
| | | | $I_O$ =250mA to750A | - | 3 | 60 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1A | | - | - | 0.5 | mA |
| | | $V_I$ = 8V to 25V | | - | - | 1.3 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 45 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 9V to 19V | | 59 | 75 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 19 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$=+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7808)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =14V, $C_I$= 0.33µF, $C_O$= 0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7808 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 7.7 | 8.0 | 8.3 | V |
| | | 5.0mA ≤ $I_O$ ≤ 1.0A, $P_O$ ≤ 15W<br>$V_I$ = 10.5V to 23V | | 7.6 | 8.0 | 8.4 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25 °C | $V_I$ = 10.5V to 25V | - | 5.0 | 160 | mV |
| | | | $V_I$ = 11.5V to 17V | - | 2.0 | 80 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C | $I_O$ = 5.0mA to 1.5A | - | 10 | 160 | mV |
| | | | $I_O$= 250mA to 750mA | - | 5.0 | 80 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | 0.05 | 0.5 | mA |
| | | $V_I$ = 10.5A to 25V | | - | 0.5 | 1.0 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 52 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz, $V_I$= 11.5V to 21.5V | | 56 | 73 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 230 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7809)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =15V, $C_I$= 0.33µF, $C_O$= 0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7809 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25°C | | 8.65 | 9 | 9.35 | V |
| | | 5.0mA≤ $I_O$ ≤1.0A, $P_O$ ≤15W<br>$V_I$= 11.5V to 24V | | 8.6 | 9 | 9.4 | |
| Line Regulation (Note1) | Regline | $T_J$=+25°C | $V_I$ = 11.5V to 25V | - | 6 | 180 | mV |
| | | | $V_I$ = 12V to 17V | - | 2 | 90 | |
| Load Regulation (Note1) | Regload | $T_J$=+25°C | $I_O$ = 5mA to 1.5A | - | 12 | 180 | mV |
| | | | $I_O$ = 250mA to 750mA | - | 4 | 90 | |
| Quiescent Current | $I_Q$ | $T_J$=+25°C | | - | 5.0 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | **mA** |
| | | $V_I$ = 11.5V to 26V | | - | - | 1.3 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -1 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 58 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 13V to 23V | | 56 | 71 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25°C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25°C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$= +25°C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7810)

(Refer to test circuit ,0°C< $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =16V, $C_I$= 0.33µF, $C_O$=0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7810 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 9.6 | 10 | 10.4 | V |
| | | 5.0mA ≤ $I_O$≤1.0A, $P_O$ ≤15W<br>$V_I$ = 12.5V to 25V | | 9.5 | 10 | 10.5 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25°C | $V_I$ = 12.5V to 25V | - | 10 | 200 | mV |
| | | | $V_I$ = 13V to 25V | - | 3 | 100 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25°C | $I_O$ = 5mA to 1.5A | - | 12 | 200 | mV |
| | | | $I_O$ = 250mA to 750mA | - | 4 | 400 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25°C | | - | 5.1 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | mA |
| | | $V_I$ = 12.5V to 29V | | - | - | 1.0 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -1 | - | mV/°C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 58 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 13V to 23V | | 56 | 71 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$=+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7812)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =19V, $C_I$= 0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7812 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 11.5 | 12 | 12.5 | V |
| | | 5.0mA ≤ $I_O$≤1.0A, $P_O$≤15W<br>$V_I$ = 14.5V to 27V | | 11.4 | 12 | 12.6 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25 °C | $V_I$ = 14.5V to 30V | - | 10 | 240 | mV |
| | | | $V_I$ = 16V to 22V | - | 3.0 | 120 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C | $I_O$ = 5mA to 1.5A | - | 11 | 240 | mV |
| | | | $I_O$ = 250mA to 750mA | - | 5.0 | 120 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.1 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | 0.1 | 0.5 | mA |
| | | $V_I$ = 14.5V to 30V | | - | 0.5 | 1.0 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -1 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 76 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 15V to 25V | | 55 | 71 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 18 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$=+25 °C | | - | 230 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ = +25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7815)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =23V, $C_I$= 0.33µF, $C_O$=0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7815 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 14.4 | 15 | 15.6 | V |
| | | 5.0mA ≤ $I_O$ ≤ 1.0A, $P_O$ ≤ 15W<br>$V_I$ = 17.5V to 30V | | 14.25 | 15 | 15.75 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25 °C | $V_I$ = 17.5V to 30V | - | 11 | 300 | mV |
| | | | $V_I$ = 20V to 26V | - | 3 | 150 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C | $I_O$ = 5mA to 1.5A | - | 12 | 300 | mV |
| | | | $I_O$ = 250mA to 750mA | - | 4 | 150 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.2 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | mA |
| | | $V_I$ = 17.5V to 30V | | - | - | 1.0 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -1 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 90 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 18.5V to 28.5V | | 54 | 70 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 19 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$=+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7818)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =27V, $C_I$= 0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7818 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 17.3 | 18 | 18.7 | V |
| | | 5.0mA ≤ $I_O$ ≤1.0A, $P_O$ ≤15W<br>$V_I$ = 21V to 33V | | 17.1 | 18 | 18.9 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25 °C | $V_I$ = 21V to 33V | - | 15 | 360 | mV |
| | | | $V_I$ = 24V to 30V | - | 5 | 180 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C | $I_O$ = 5mA to 1.5A | - | 15 | 360 | mV |
| | | | $I_O$ = 250mA to 750mA | - | 5.0 | 180 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.2 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | mA |
| | | $V_I$ = 21V to 33V | | - | - | 1 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -1 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 110 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 22V to 32V | | 53 | 69 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 22 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$=+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7824)

(Refer to test circuit ,0°C < $T_J$ < 125°C, $I_O$ = 500mA, $V_I$ =33V, $C_I$= 0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | MC7824 | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 23 | 24 | 25 | V |
| | | 5.0mA ≤ $I_O$ ≤ 1.0A, $P_O$ ≤ 15W<br>$V_I$ = 27V to 38V | | 22.8 | 24 | 25.25 | |
| Line Regulation (Note1) | Regline | $T_J$ =+25 °C | $V_I$ = 27V to 38V | - | 17 | 480 | mV |
| | | | $V_I$ = 30V to 36V | - | 6 | 240 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C | $I_O$ = 5mA to 1.5A | - | 15 | 480 | mV |
| | | | $I_O$ = 250mA to 750mA | - | 5.0 | 240 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.2 | 8.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1.0A | | - | 0.1 | 0.5 | mA |
| | | $V_I$ = 27V to 38V | | - | 0.5 | 1 | |
| Output Voltage Drift | $\Delta V_O/\Delta T$ | $I_O$ = 5mA | | - | -1.5 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz, $T_A$ =+25 °C | | - | 60 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz<br>$V_I$ = 28V to 38V | | 50 | 67 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$=+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 28 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$ = 35V, $T_A$=+25 °C | | - | 230 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$ =+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Changes in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7805A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 10V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 4.9 | 5 | 5.1 | V |
| | | $I_O$ = 5mA to 1A, $P_O \leq$ 15W<br>$V_I$ = 7.5V to 20V | | 4.8 | 5 | 5.2 | |
| Line Regulation (Note1) | Regline | $V_I$ = 7.5V to 25V<br>$I_O$ = 500mA | | - | 5 | 50 | mV |
| | | $V_I$ = 8V to 12V | | - | 3 | 50 | |
| | | $T_J$ =+25 °C | $V_I$= 7.3V to 20V | - | 5 | 50 | |
| | | | $V_I$= 8V to 12V | - | 1.5 | 25 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 9 | 100 | mV |
| | | $I_O$ = 5mA to 1A | | - | 9 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 4 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 6 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1A | | - | - | 0.5 | mA |
| | | $V_I$ = 8 V to 25V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $V_I$ = 7.5V to 20V, $T_J$ =+25 °C | | - | - | 0.8 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | Io = 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 8V to 18V | | - | 68 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$= +25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7806A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ =11V, $C_I$=0.33µF, $C_O$=0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 5.58 | 6 | 6.12 | V |
| | | $I_O$ = 5mA to 1A, $P_O \leq$ 15W<br>$V_I$ = 8.6V to 21V | | 5.76 | 6 | 6.24 | |
| Line Regulation (Note1) | Regline | $V_I$= 8.6V to 25V<br>$I_O$ = 500mA | | - | 5 | 60 | mV |
| | | $V_I$= 9V to 13V | | - | 3 | 60 | |
| | | $T_J$ =+25 °C | $V_I$= 8.3V to 21V | - | 5 | 60 | |
| | | | $V_I$= 9V to 13V | - | 1.5 | 30 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 9 | 100 | mV |
| | | $I_O$ = 5mA to 1A | | - | 4 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 5.0 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 4.3 | 6 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1A | | - | - | 0.5 | mA |
| | | $V_I$ = 9V to 25V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $V_I$= 8.5V to 21V, $T_J$ =+25 °C | | - | - | 0.8 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 9V to 19V | | - | 65 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7808A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 14V, $C_I$=0.33µF, $C_O$=0.1µF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 7.84 | 8 | 8.16 | V |
| | | $I_O$ = 5mA to 1A, $P_O$ ≤15W<br>$V_I$ = 10.6V to 23V | | 7.7 | 8 | 8.3 | |
| Line Regulation (Note1) | Regline | $V_I$= 10.6V to 25V<br>$I_O$ = 500mA | | - | 6 | 80 | mV |
| | | $V_I$= 11V to 17V | | - | 3 | 80 | |
| | | $T_J$ =+25 °C | $V_I$= 10.4V to 23V | - | 6 | 80 | |
| | | | $V_I$= 11V to 17V | - | 2 | 40 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 12 | 100 | mV |
| | | $I_O$ = 5mA to 1A | | - | 12 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 5 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 6 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $I_O$ = 5mA to 1A | | - | - | 0.5 | mA |
| | | $V_I$ = 11V to 25V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $V_I$= 10.6V to 23V, $T_J$ =+25 °C | | - | - | 0.8 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -0.8 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | µV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 11.5V to 21.5V | | - | 62 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 18 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7809A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 15V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25°C | | 8.82 | 9.0 | 9.18 | V |
| | | $I_O$ = 5mA to 1A, $P_O$≤15W<br>$V_I$ = 11.2V to 24V | | 8.65 | 9.0 | 9.35 | |
| Line Regulation (Note1) | Regline | $V_I$= 11.7V to 25V<br>$I_O$ = 500mA | | - | 6 | 90 | mV |
| | | $V_I$= 12.5V to 19V | | - | 4 | 45 | |
| | | $T_J$ =+25°C | $V_I$= 11.5V to 24V | - | 6 | 90 | |
| | | | $V_I$= 12.5V to 19V | - | 2 | 45 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25°C<br>$I_O$ = 5mA to 1.0A | | - | 12 | 100 | mV |
| | | $I_O$ = 5mA to 1.0A | | - | 12 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 5 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $V_I$ = 11.7V to 25V, $T_J$=+25 °C | | - | - | 0.8 | mA |
| | | $V_I$ = 12V to 25V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -1.0 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 12V to 22V | | - | 62 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2.0 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25°C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant, junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7810A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 16V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25°C | | 9.8 | 10 | 10.2 | V |
| | | $I_O$ = 5mA to 1A, $P_O \leq$ 15W<br>$V_I$ =12.8V to 25V | | 9.6 | 10 | 10.4 | |
| Line Regulation (Note1) | Regline | $V_I$= 12.8V to 26V<br>$I_O$ = 500mA | | - | 8 | 100 | mV |
| | | $V_I$= 13V to 20V | | - | 4 | 50 | |
| | | $T_J$ =+25 °C | $V_I$= 12.5V to 25V | - | 8 | 100 | |
| | | | $V_I$= 13V to 20V | - | 3 | 50 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 12 | 100 | mV |
| | | $I_O$ = 5mA to 1.0A | | - | 12 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 5 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.0 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $V_I$ = 13V to 26V, $T_J$=+25 °C | | - | - | 0.5 | mA |
| | | $V_I$ = 12.8V to 25V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -1.0 | - | mV/°C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 14V to 24V | | - | 62 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25°C | | - | 2.0 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 17 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7812A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 19V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 11.75 | 12 | 12.25 | V |
| | | $I_O$ = 5mA to 1A, $P_O$ ≤15W<br>$V_I$ = 14.8V to 27V | | 11.5 | 12 | 12.5 | |
| Line Regulation (Note1) | Regline | $V_I$= 14.8V to 30V<br>$I_O$ = 500mA | | - | 10 | 120 | mV |
| | | $V_I$= 16V to 22V | | - | 4 | 120 | |
| | | $T_J$ =+25 °C | $V_I$= 14.5V to 27V | - | 10 | 120 | |
| | | | $V_I$= 16V to 22V | - | 3 | 60 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 12 | 100 | mV |
| | | $I_O$ = 5mA to 1.0A | | - | 12 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 5 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25°C | | - | 5.1 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $V_I$ = 15V to 30V, $T_J$=+25 °C | | - | | 0.8 | mA |
| | | $V_I$ = 14V to 27V, $I_O$ = 500mA | | - | | 0.8 | |
| | | $I_O$ = 5mA to 1.0A | | - | | 0.5 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -1.0 | - | mV/°C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25°C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 14V to 24V | | - | 60 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25°C | | - | 2.0 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 18 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7815A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ =23V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 14.7 | 15 | 15.3 | V |
| | | $I_O$ = 5mA to 1A, $P_O$ ≤15W<br>$V_I$ = 17.7V to 30V | | 14.4 | 15 | 15.6 | |
| Line Regulation (Note1) | Regline | $V_I$= 17.9V to 30V<br>$I_O$ = 500mA | | - | 10 | 150 | mV |
| | | $V_I$= 20V to 26V | | - | 5 | 150 | |
| | | $T_J$ =+25°C | $V_I$= 17.5V to 30V | - | 11 | 150 | |
| | | | $V_I$= 20V to 26V | - | 3 | 75 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 12 | 100 | mV |
| | | $I_O$ = 5mA to 1.0A | | - | 12 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 5 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $V_I$ = 17.5V to 30V, $T_J$ =+25 °C | | - | - | 0.8 | mA |
| | | $V_I$ = 17.5V to 30V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -1.0 | - | mV/°C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25 °C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 18.5V to 28.5V | | - | 58 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2.0 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 19 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25°C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7818A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 27V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 17.64 | 18 | 18.36 | V |
| | | $I_O$ = 5mA to 1A, $P_O$ ≤15W<br>$V_I$ = 21V to 33V | | 17.3 | 18 | 18.7 | |
| Line Regulation (Note1) | Regline | $V_I$= 21V to 33V<br>$I_O$ = 500mA | | - | 15 | 180 | mV |
| | | $V_I$= 21V to 33V | | - | 5 | 180 | |
| | | $T_J$ =+25 °C | $V_I$= 20.6V to 33V | - | 15 | 180 | |
| | | | $V_I$= 24V to 30V | - | 5 | 90 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25°C<br>$I_O$ = 5mA to 1.5A | | - | 15 | 100 | mV |
| | | $I_O$ = 5mA to 1.0A | | - | 15 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 7 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $V_I$ = 21V to 33V, $T_J$=+25 °C | | - | - | 0.8 | mA |
| | | $V_I$ = 21V to 33V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -1.0 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ =+25°C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 22V to 32V | | - | 57 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25°C | | - | 2.0 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 19 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25°C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in $V_O$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.

## Electrical Characteristics (MC7824A)

(Refer to the test circuits. 0°C < $T_J$ < 125°C, $I_O$ =1A, $V_I$ = 33V, $C_I$=0.33μF, $C_O$=0.1μF, unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | $T_J$ =+25 °C | | 23.5 | 24 | 24.5 | V |
| | | $I_O$ = 5mA to 1A, $P_O$ ≤15W<br>$V_I$ = 27.3V to 38V | | 23 | 24 | 25 | |
| Line Regulation (Note1) | Regline | $V_I$= 27V to 38V<br>$I_O$ = 500mA | | - | 18 | 240 | mV |
| | | $V_I$= 21V to 33V | | - | 6 | 240 | |
| | | $T_J$ =+25 °C | $V_I$= 26.7V to 38V | - | 18 | 240 | |
| | | | $V_I$= 30V to 36V | - | 6 | 120 | |
| Load Regulation (Note1) | Regload | $T_J$ =+25 °C<br>$I_O$ = 5mA to 1.5A | | - | 15 | 100 | mV |
| | | $I_O$ = 5mA to 1.0A | | - | 15 | 100 | |
| | | $I_O$ = 250mA to 750mA | | - | 7 | 50 | |
| Quiescent Current | $I_Q$ | $T_J$ =+25 °C | | - | 5.2 | 6.0 | mA |
| Quiescent Current Change | $\Delta I_Q$ | $V_I$ = 27.3V to 38V, $T_J$ =+25 °C | | - | - | 0.8 | mA |
| | | $V_I$ = 27.3V to 38V, $I_O$ = 500mA | | - | - | 0.8 | |
| | | $I_O$ = 5mA to 1.0A | | - | - | 0.5 | |
| Output Voltage Drift | $\Delta V/\Delta T$ | $I_O$ = 5mA | | - | -1.5 | - | mV/ °C |
| Output Noise Voltage | $V_N$ | f = 10Hz to 100KHz<br>$T_A$ = 25 °C | | - | 10 | - | μV/Vo |
| Ripple Rejection | RR | f = 120Hz, $I_O$ = 500mA<br>$V_I$ = 28V to 38V | | - | 54 | - | dB |
| Dropout Voltage | $V_{Drop}$ | $I_O$ = 1A, $T_J$ =+25 °C | | - | 2.0 | - | V |
| Output Resistance | $r_O$ | f = 1KHz | | - | 20 | - | mΩ |
| Short Circuit Current | $I_{SC}$ | $V_I$= 35V, $T_A$ =+25 °C | | - | 250 | - | mA |
| Peak Current | $I_{PK}$ | $T_J$=+25 °C | | - | 2.2 | - | A |

**Note:**

1. Load and line regulation are specified at constant junction temperature. Change in VO due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# Typical Perfomance Characteristics

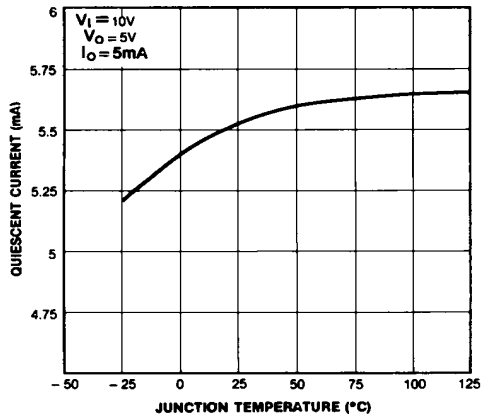



Figure 1. Quiescent Current

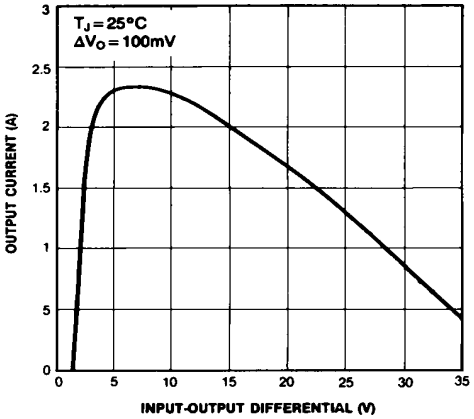



Figure 2. Peak Output Current

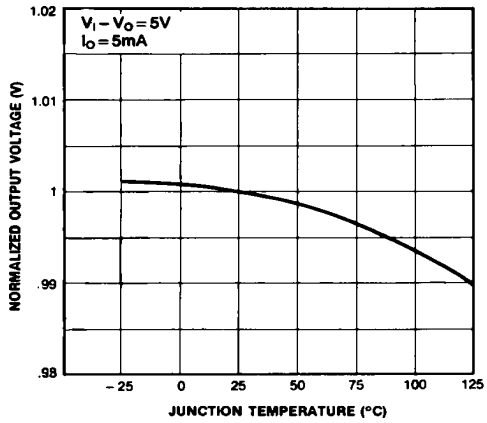



Figure 3. Output Voltage

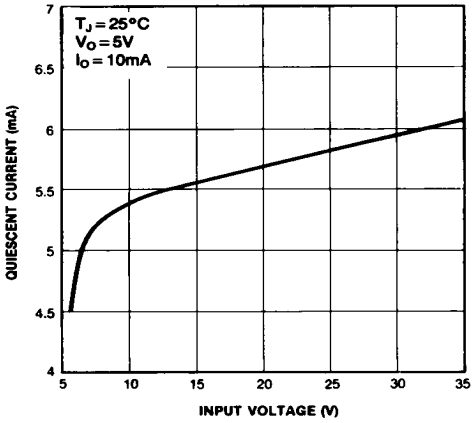



Figure 4. Quiescent Current

# Typical Applications

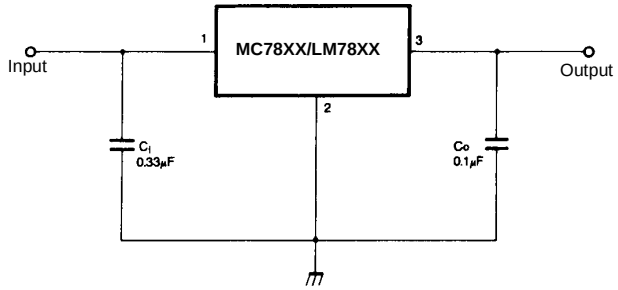



**Figure 5. DC Parameters**

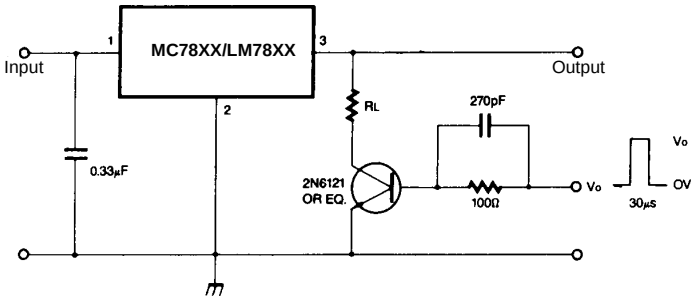



**Figure 6. Load Regulation**

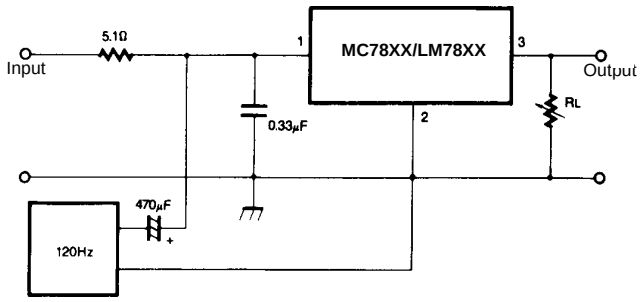



**Figure 7. Ripple Rejection**

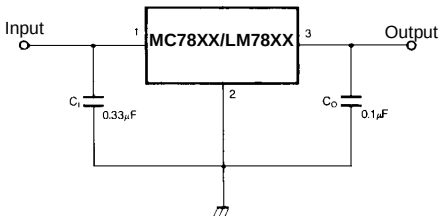



**Figure 8. Fixed Output Regulator**

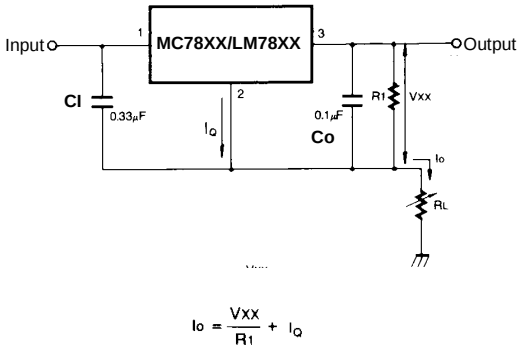


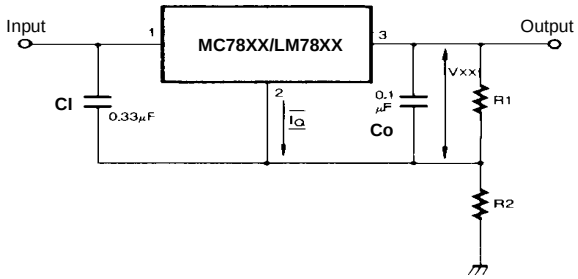

**Figure 9. Constant Current Regulator**

**Notes**:

(1) To specify an output voltage. substitute voltage value for "XX." A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

(2) $C_I$ is required if regulator is located an appreciable distance from power Supply filter.

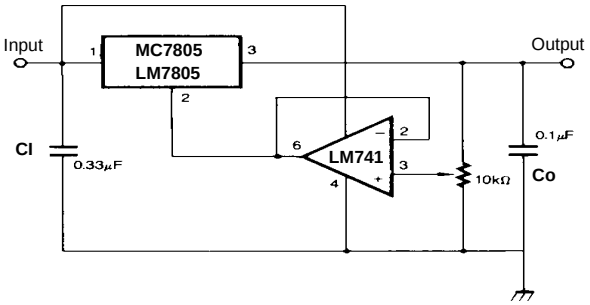
(3) $C_O$ improves stability and transient response.




$$I_{RI} \geq 5IQ$$

$$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$$

**Figure 10. Circuit for Increasing Output Voltage**




$$I_{RI} \geq 5\ I_Q$$

$$V_O = V_{XX}(1+R_2/R_1)+I_QR_2$$

**Figure 11. Adjustable Output Regulator (7 to 30V)**

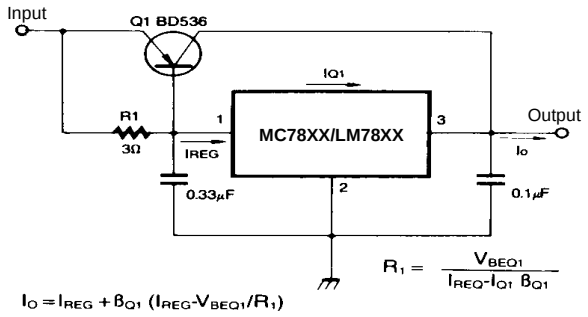



**Figure 12. High Current Voltage Regulator**

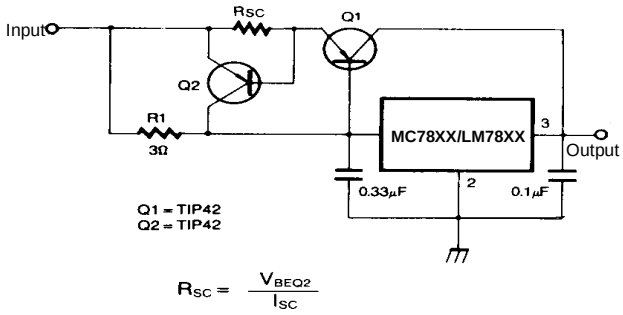



**Figure 13. High Output Current with Short Circuit Protection**

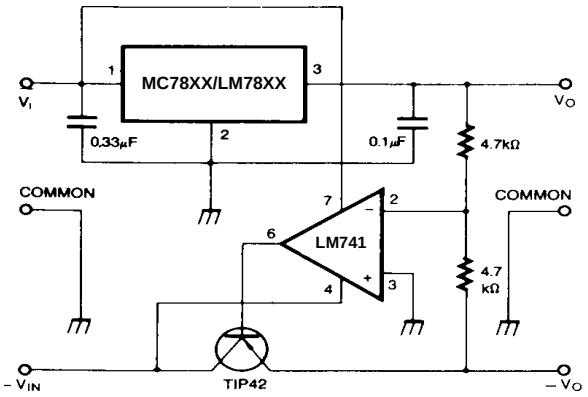



**Figure 14. Tracking Voltage Regulator**

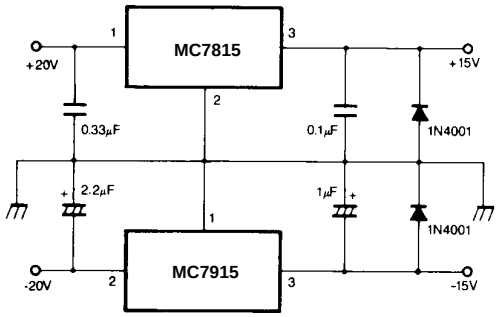



**Figure 15. Split Power Supply ( ±15V-1A)**

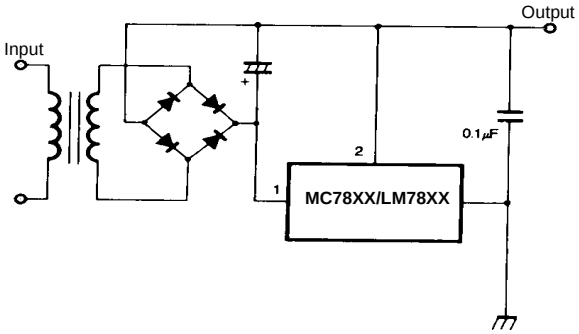



**Figure 16. Negative Output Voltage Circuit**

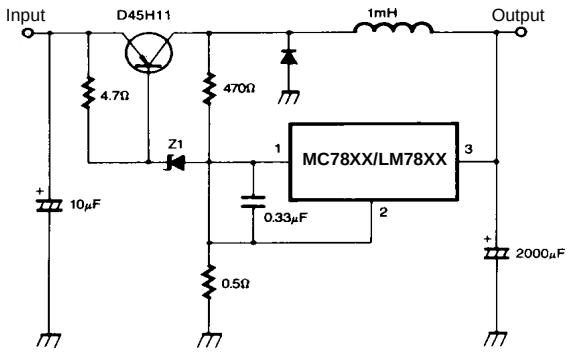
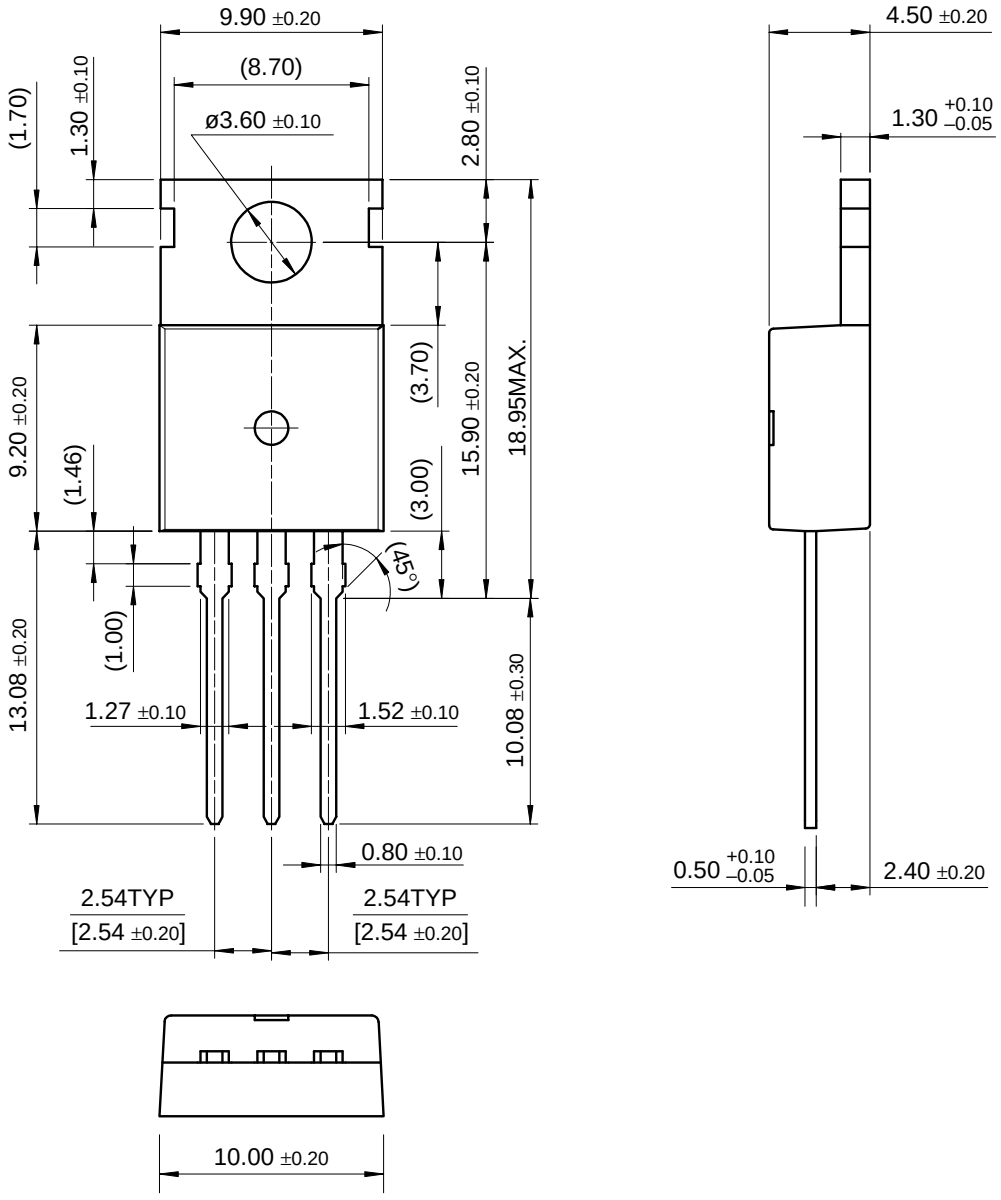



**Figure 17. Switching Regulator**

# Mechanical Dimensions

## Package

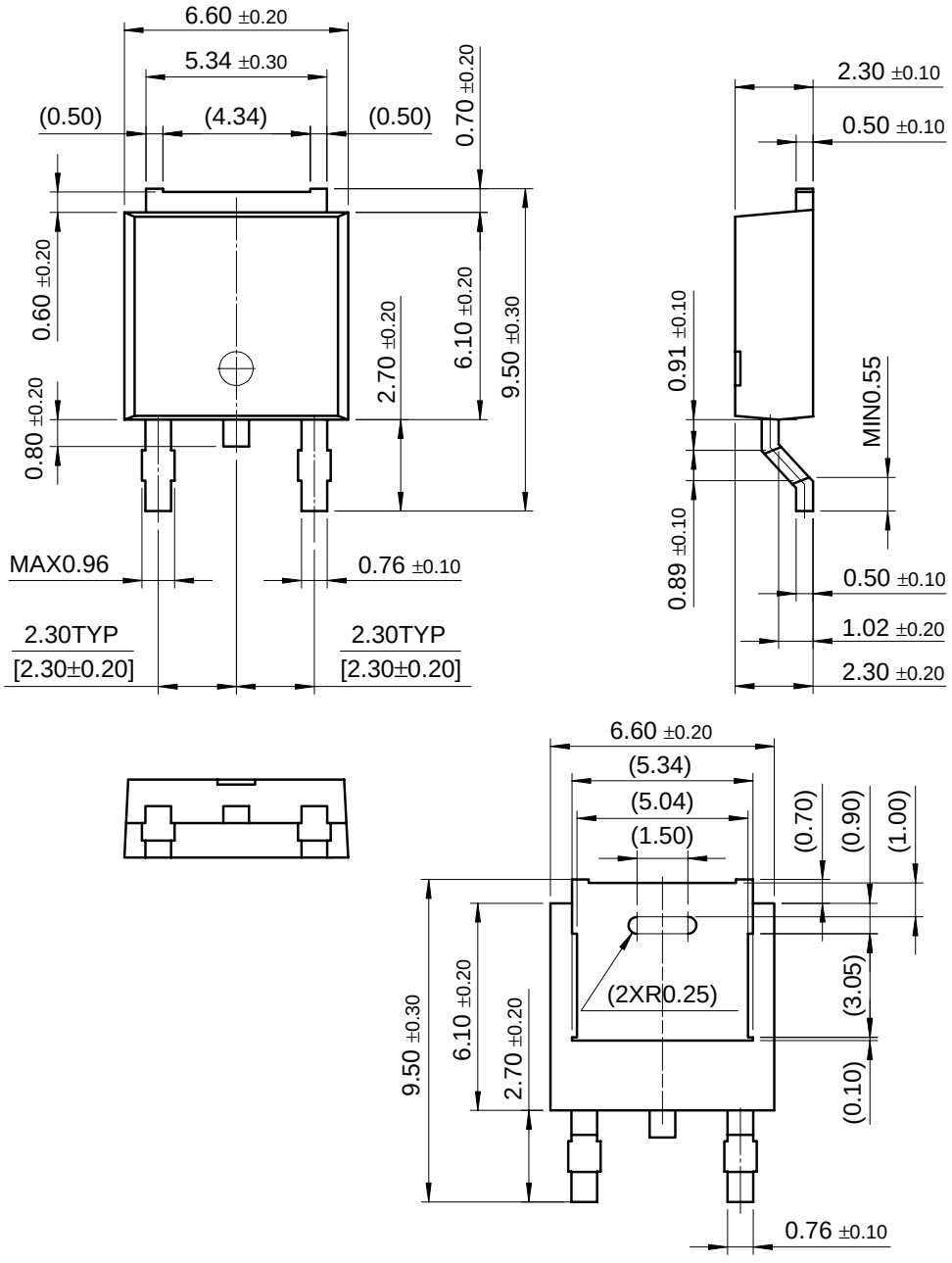
### TO-220



## Mechancal Dimensions (Continued)

### Package

# D-PAK



## Ordering Information

| Product Number | Output Voltage Tolerance | Package | Operating Temperature |
|---|---|---|---|
| LM7805CT | ±4% | TO-220 | 0 ~ + 125°C |

| Product Number | Output Voltage Tolerance | Package | Operating Temperature |
|---|---|---|---|
| MC7805CT | ±4% | TO-220 | 0 ~ + 125°C |
| MC7806CT | | | |
| MC7808CT | | | |
| MC7809CT | | | |
| MC7810CT | | | |
| MC7812CT | | | |
| MC7815CT | | | |
| MC7818CT | | | |
| MC7824CT | | | |
| MC7805CDT | | D-PAK | |
| MC7806CDT | | | |
| MC7808CDT | | | |
| MC7809CDT | | | |
| MC7810CDT | | | |
| MC7812CDT | | | |
| MC7805ACT | ±2% | TO-220 | |
| MC7806ACT | | | |
| MC7808ACT | | | |
| MC7809ACT | | | |
| MC7810ACT | | | |
| MC7812ACT | | | |
| MC7815ACT | | | |
| MC7818ACT | | | |
| MC7824ACT | | | |